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### Active Isolatid

#### **QHx220**

Electromagnetic Interference (EMI) is emerging as a major concern in next generation wireless communication systems. As wireless terminals now support multiple services and features that utilize high data rates simultaneously, removing interference within wireless terminals like handsets has become a challenge.

Reducing the Electromagnetic Interference recovers the receiver sensitivity, enabling simultaneous operation of multiple radios, and improves the overall quality of service of communication devices. Intersil's QHx220 is situated in a handset to sample the source of the noise and emulate the RF coupling channel between the noise source and victim receiver antenna. In doing so, an anti-noise signal can be applied directly to the victim receive path to cancel the EMI and achieve the signal integrity benefits. This approach makes it possible to cancel both in-band (within the victim Rx band) or out-of-band aggressors. This is a revolutionary approach since it is only possible to cancel out of band noise using conventional Rx filters.

In addition QHx220 may be used to increase the inherent isolation between antennas or inside duplexers and switches, thus allowing to increase the transmit power in repeaters or yielding higher sensitivity in the receivers. Both measures finally resulting in a better coverage, larger cell size, smaller antennas or lower power of infrastructure components such as basestations, pico-and Femtocells as well as repeaters.

The QHx220 integrates the sampler path LNA gain stages as well as the DACs required to control the I and Q control voltages (used to set the magnitude and phase of the cancellation signal). Both the gain, and control voltages are programmable using a SPI bus interface.

#### **Features**

- Protocol agnostic. Designed for: GSM, CDMA, DVB-H, ISDB-T, DMB
- Frequency Range 300MHz to 3GHz
- Integrated, programmable LNA gain stages in the sampler path
- SPI bus controlled integrated DACs
- >20dB Noise Cancellation is possible
- 50dB typical Dynamic Range
- Low Power Consumption (<20mW typical, ~2μW standby)</li>
- Ultra Small ~ 1mm<sup>2</sup> devices are available as tested bumped die or 3x3mm<sup>2</sup> QFN package

### **Applications**

- · Most any wireless device with a local aggressor:
  - Cell phones
  - Mobile TV devices
  - Laptop Computers
  - GPS terminals
  - Pico- and Femtocells
- Improved Tx to Rx Isolation of devices (i.e. duplexer, switches) or between neighboring antennae
- Basestations
- · Linearization of PAs

### **Typical Application Circuit**

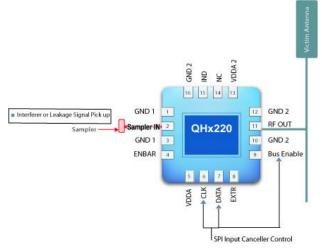


FIGURE 1. ACTIVE ISOLATION ENHANCER AND NOISE CANCELLER

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#### **Benefits**

- · Actively cancels unwanted local RF noise
- Improves BER, receiver sensitivity, C/N by canceling noise generated from local aggressors
- Improves isolation between adjacent antennas
- Can be used to cancel in-band or out-of-band interferers (i.e. spurs, harmonics, phase noise, or other noise sources like IM products generated in a PA)
- Enables simultaneous operation of multiple co-located radios
- · Improves overall quality of service

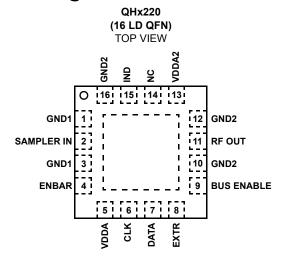
### **Ordering Information**

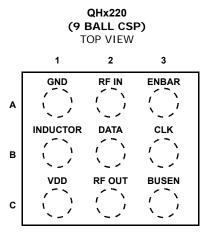
PART NUMBER (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
QHX220IQT7	QH220	-40 to +85	16 Ld QFN 7" Prod. Tape & Reel; Qty 1,000	L16.3x3B
QHX220IQSR	QH220	-40 to +85	16 Ld QFN 7" Sample Reel; Qty 100	L16.3x3B
Coming Soon QHX220ICT7 (Note 2)	220	-40 to +85	9 Ball CSP 7" Prod. Tape & Reel; Qty 1,000	TBD
Coming Soon QHX220ICSR (Note 2)	220	-40 to +85	9 Ball CSP 7" Sample Reel; Qty 100	TBD

#### NOTES:

- 1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- 2. Contact Intersil Marketing for availability.

### **Pin Configurations**





### **Pin Descriptions**

QFN PIN #	QFN PIN NAME	CSP PIN #	CSP PIN NAME	DESCRIPTION
1, 3, 10, 12, 16	GNDx	1A	GND	Ground
2	SAMPLER IN	2A	RF IN	RF Input
4	ENBAR	3A	ENBAR	Enable (active low) → Tied to GND
5, 13	VDDx	1C	VDD	1.8V Power Supply
6	CLK	3B	CLK	Input Clock (SPI)
7	DATA	2B	DATA	Data Line (SPI)
8	EXTR	-	-	External Resistor for Gain Tempco Control
9	BUS ENABLE	3C	BUSEN	Bus Enable (active low, SPI)
11	RF OUT	2C	RF OUT	RF Output
14	NC	-	-	No Connect
15	IND	1B	INDUCTOR	External Inductor for LNA
-	Exposed Center Pad	-	-	Ground

### Overcoming Noise or Interference Using the QHx220

#### Identifying Common Sources of Electromagnetic Interference (EMI)

- A flex cable carrying high-speed data from a base-band processor to an LCD/Camera display.
- Closely spaced antennas of radios operating simultaneously.
- Harmonics, other mixing products or spurs that fall within the victim receive band.
- Poor isolation from local transmitter (via antennas, duplexers or other front end modules).
- Noise on common Ground or V<sub>CC</sub> supply lines.

### Acquiring and Sampling the Source of Unwanted Interference

Intersil's QHx220 reduces EMI by sampling the interference source at its input. The sampled noise signal is acquired in close proximity to the noise source either with an EMI detector, an additional coupling element on the PCB or direct tap of the noise source using a RC network.

## **Emulating the Coupling Channel to Achieve an Inverse Signal**

Once the QHx220 acquires and samples the unwanted interferer, the general-purpose canceller feeds the sampled noise signal through an analog signal processor, which allows control of the phase within 360° and the amplitude within a dynamic range of 50dB. This enables the QHx220 to output an inverse signal of the interference plus coupling channel in order to eliminate the desensitization of the victim receiver.

#### **Absolute Maximum Ratings**

#### I/O Voltage at All Input Pins $\ \ldots \ .$ GND - 0.3V to VDD + 0.3V ESD Rating (HBM) . . . . . . . . . 2kV

#### **Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
16 Ld QFN Package (Notes 3, 4) .	. 60	13
Operating Ambient Temperature Ran	ge40	°C to +85°C
Storage Ambient Temperature Range	e55°	C to +150°C
Maximum Junction Temperature		+125°C
Pb-free reflow profile	S	ee link below
http://www.intersil.com/pbfree/Pb	-FreeReflow.	<u>asp</u>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

- 3.  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- 4. For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

### **Operating Conditions**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	$V_{DD}$		1.7	1.8	1.9	V	
Operating Ambient Temperature	T <sub>A</sub>		-40	25	85	°C	
Power Consumption (operation mode)		@high/low gain mode		16	28.7	mW	5
		@boost gain mode		23	33	mW	5
Power Consumption (standby mode)				10	38.3	μW	5

#### NOTE:

5. Max Power specifications tested under ECC test conditions.

### **Control Pin Characteristics**

Typical values are at  $V_{DD} = 1.8V$ ,  $T_A = +25$ °C, and  $P_{IN} = < -48$ dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD}=1.7V$  to 1.9V,  $T_A=-40^{\circ}C$  to  $+85^{\circ}C$ .

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Logic Input Level - Low	ENBAR low				0.2 V <sub>DD</sub>	mV	
Logic Input Level - High	ENBAR high		0.8 V <sub>DD</sub>			V	
Enable Response Time		Delay following high to low transition until RF output is within 10% of its final value.		535		ns	6
Disable Response Time		Delay following low to high transition until RF output is within 10% of its final value.		350		ns	
Control Word Length				24		Bits	
Bits 0-9		I-DAC value		10		Bits	
Bits 10-19		Q-DAC value		10		Bits	
Bits 20-21		Application select					
		00: UHF-Band					
		01: L-Band					
		11: ISM Band					
Bit 22		Gain Switch		1		Bit	
Bit 23 (Note 18)		Extended Feature		1		Bit	7

#### NOTES:

- 6. The enable response time is bounded by the input AC cap on board. Typical response time reflects 100pF capacitance.
- 7. Generally set to low. Two successive SPI instructions are needed to enable or disable boost gain mode.

Sequence to enable boost gain mode → 1st instruction: set Bit<23:20> to 1x01'b

→ 2nd instruction: set Bit<23:20> to 0xxx'b

Sequence to disable boost gain mode → 1st instruction: set Bit<23:20> to 1x10'b

→ 2nd instruction: set Bit<23:20> to 0xxx'b

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### **SPI Bus Characteristics**

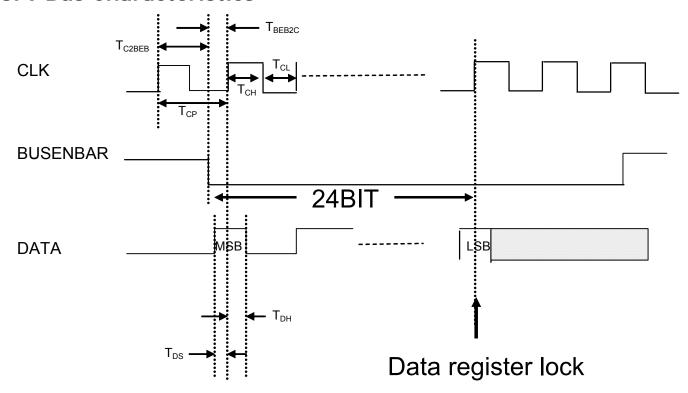


FIGURE 2. SPI BUS TIMING DIAGRAM

#### SPI BUS TIMING REQUIREMENT

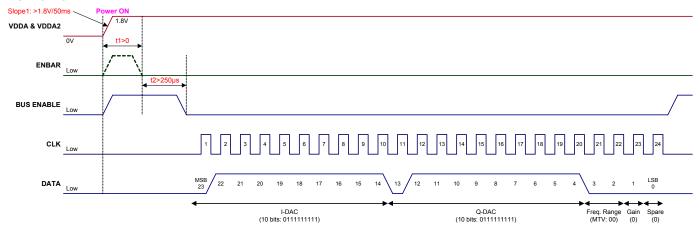
SYMBOL	PARAMETER	MIN	TYP	MAX
t <sub>CP</sub>	SPI clock period	100ns		
t <sub>CL</sub>	Clock pulse width low	40ns		
t <sub>CH</sub>	Clock pulse width high	40ns		
t <sub>BEB2C</sub>	BUSENBAR Fall to CLK Rise Setup Time	5ns		
t <sub>C2BEB</sub>	CLK Rise BUSENBAR Fall Delay	40ns		
t <sub>DS</sub>	Data Setup Time	20ns		
t <sub>DH</sub>	Data Hold Time	0ns		

#### TABLE 1. SPI BUS DATA FORMAT

10BIT I-DAC	10BIT Q-DAC	FREQ RANGE	GAIN	SPARE
<23:14>	<13:4>	<3:2>	<1>	<0>

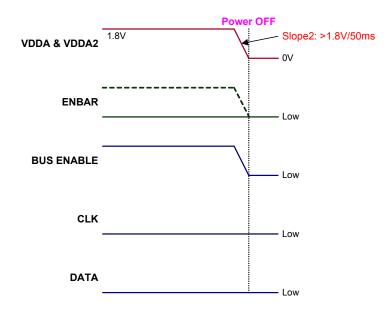
### Power ON/OFF Sequence

#### **Power ON**



(This command sets QHx220 into minimum gain (Note 8))

#### **Power OFF**



#### NOTES:

- 8. When the chip is powered up its register are all zero. This means -135° phase and full analog gain, WLAN Application and 0dB coarse gain (the boost gain mode is not enabled).
- 9. VDDA and VDDA2 should be connected on the PCB and decoupled with caps right next to the pin.
- 10. The SPI Bus is not accessible when VDDA/VDDA2 are <1V.

#### **Electrical Specifications**

Typical test conditions (TTC)  $V_{DD}=1.8V$ ,  $T_A=+25^{\circ}C$ , and PIN < -48 dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD}=1.7V$  to 1.9V,  $T_A=-40^{\circ}C$  to  $+85^{\circ}$ C. Output load test condition is  $50\Omega$  in parallel with  $50\Omega$  unless otherwise stated. Electrical specifications reflect performance of QFN packaged devices.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Frequency Coverage		0.3		3	GHz	11
Max. Gain (high gain mode)	UHF-Band 450MHz/770MHz	8.4/-3	14.9/8.0	18/11.8	dB	12
	L-Band 1575MHz	7.3	12.0	16.3	dB	12
	ISM Band 2400MHz		2.0		dB	12
Max. Gain (low gain mode)	UHF-Band 450MHz/770MHz	-7.2/-15.4	2.8/-4.1	7.3/1.4	dB	12
	L-Band 1575MHz	-5.4	0.9	4.9	dB	12
	ISM Band 2400MHz		-9.1		dB	12
Max. Gain (Boost gain mode)	UHF-Band 450MHz/770MHz	17.1/9.2	20.1/12.2	23.1/15.2	dB	12
	L-Band 1575MHz	14.7	17.7	20.7	dB	12
	ISM Band 2400MHz		7.64		dB	12
Max Dynamic Range		27.4	50		dB	
Phase Control Range		0		360	0	
Absolute Gain Accuracy over	UHF-Band 450MHz/770MHz	-2.5		1.5	dB	13, 18
ECC	L-Band 1575MHz	-2.5		1.5	dB	13, 18
	ISM Band 2400MHz				dB	13, 18
IIP3 of Sampler Input	UHF-Band 450MHz/770MHz		-34.7/-24.7		dBm	18
(high gain mode)	L-Band 1575MHz	-34.8	-31.3		dBm	18
	ISM Band 2400MHz		-20.75		dBm	18
IIP3 of Sampler Input	UHF-Band 450MHz/770MHz		-33.4/-25.1		dBm	18
(low gain mode)	L-Band 1575MHz	-35.1	-31.5		dBm	18
	ISM Band 2400MHz		-23		dBm	18
IIP3 of Sampler Input	UHF-Band 450MHz/770MHz	-46.3/-34.5	-42.8/-31.0		dBm	18
(Boost high gain mode)	L-Band 1575MHz	-40.48	-36.98		dBm	18
	ISM Band 2400MHz		-24		dBm	18
Output Noise Power	UHF-Band 450MHz/770MHz		-158.8/-164.1		dBm/Hz	14, 18
(high gain mode)	L-Band 1575MHz		-161.7		dBm/Hz	14, 18
	ISM Band 2400MHz		-168.7		dBm/Hz	14, 18
Output Noise Power	UHF-Band 450MHz/770MHz		-168.6/-171.6		dBm/Hz	14, 18
(low gain mode)	L-Band 1575MHz		-169.8		dBm/Hz	14, 18
	ISM Band 2400MHz		-173.1		dBm/Hz	14, 18
Output Noise Power	UHF-Band 450MHz/770MHz		-153.9/-160.5		dBm/Hz	14, 18
(Boost high gain mode)	L-Band 1575MHz		-156.1		dBm/Hz	14, 18
	ISM Band 2400MHz		-164.7		dBm/Hz	14, 18
LNA Noise Figure (high gain	UHF-Band 450MHz/770MHz		1.5		dBm	15, 18
mode)	L-Band 1575MHz		1.5		dBm	15, 18
	ISM Band 2400MHz		2.0		dBm	15, 18

#### **Electrical Specifications**

Typical test conditions (TTC)  $V_{DD}=1.8V$ ,  $T_A=+25^{\circ}C$ , and PIN < -48 dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD}=1.7V$  to 1.9V,  $T_A=-40^{\circ}C$  to +85°C. Output load test condition is  $50\Omega$  in parallel with  $50\Omega$  unless otherwise stated. Electrical specifications reflect performance of QFN packaged devices. (Continued)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Reflection Coefficient	UHF-Band 450MHz/770MHz		-1.0/-2.6		dBm	15, 18
(high gain)	L-Band 1575MHz		-0.06		dBm	15, 18
	ISM Band 2400MHz		-2.3		dBm	15, 18
Input Reflection Coefficient (low gain)	UHF-Band 450MHz/770MHz		-1.3/-2.5		dB	16, 18
	L-Band 1575MHz		-0.3		dB	16, 18
	ISM Band 2400MHz		-2.1		dB	16, 18
Input Reflection Coefficient	UHF-Band 450MHz/770MHz		-1.0/-2.7		dB	16, 18
(Boost high gain)	L-Band 1575MHz		2.4		dB	16, 18
	ISM Band 2400MHz		-1.0		dB	16, 18
RF Output Impedance (Rp//Cp)	UHF-Band 450MHz/770MHz		Rp = 6.9/4.6, Cp = 620/616		kΩ, fF	17, 18
	L-Band 1575MHz		Rp = 2.2, Cp = 619		kΩ, fF	17, 18
	ISM Band 2400MHz		Rp = 1.0, Cp = 680		kΩ, fF	17, 18
Output Insertion Loss	UHF-Band 450MHz/770MHz		0.1		dB	18
	L-Band 1575MHz		0.3		dB	18
	ISM Band 2400MHz		0.7		dB	18

#### NOTES:

- 11. Part will operate under the specified frequency ranges. Electrical performance is not optimal beyond the UHF-Band (low end) and ISM Band (high end).
- 12. Data provided for external tank circuit with Q=2 and  $f_{center}\!\!\approx\!\!550 MHz.$
- 13. Extreme corner conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40$ °C to +85°C.
- 14. Input connected to a  $50\Omega$  load during measurement.
- 15. NF improves beyond high gain when going into boost gain. Values not tested on ATE.
- 16. S11 based upon single series inductor matching.
- 17. Rp//Cp given at typical gain point of canceller.
- 18. Limits established by characterization and not production tested.

### **Typical Performance Characteristics (UHF-Band)**

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and PIN < -48dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

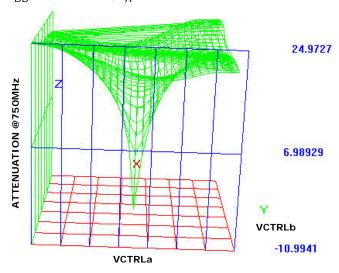


FIGURE 3. 3D ATTENUATION PLOT FOR GAIN AND PHASE FAMILY OF CURVES

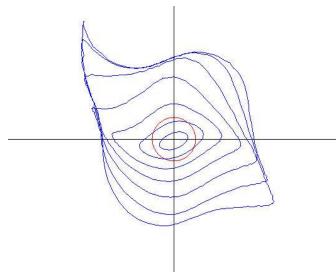


FIGURE 4. 2D CONTOUR PLOT FOR GAIN AND PHASE FAMILY OF CURVES IN HIGH BOOST MODE (RED CIRCLE = UNITY GAIN)



FIGURE 5. GAIN vs FREQUENCY AT LOW, MID, HIGH, AND BOOST GAIN SET POINTS

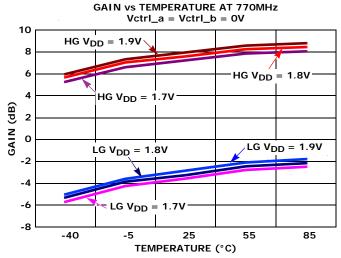


FIGURE 6. GAIN VARIATION UNDER ECC MEASURED
AT 770MHz AT MAX GAIN SET-POINT

### Typical Performance Characteristics (UHF-Band) (Continued)

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and PIN < -48dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

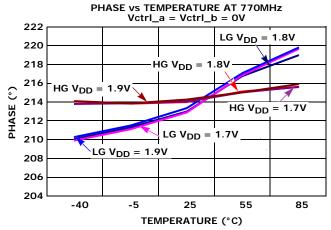


FIGURE 7. PHASE VARIATION UNDER ECC MEASURED
AT 770MHz AT MAX GAIN SET-POINT

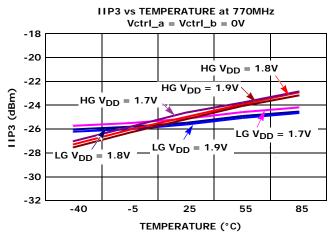


FIGURE 8. IIP3 VARIATION UNDER ECC MEASURED AT 770MHz AT MAX GAIN SET-POINT

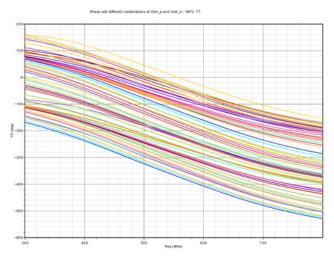


FIGURE 9. PHASE COVERAGE FOR GAIN AND PHASE FAMILY OF CURVES

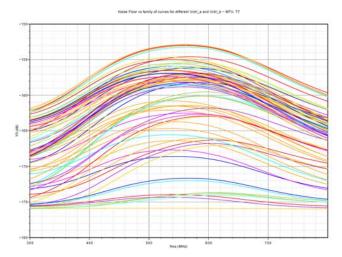
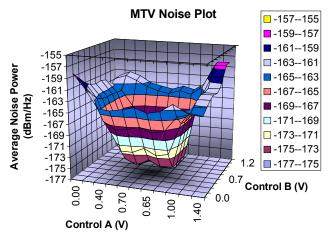


FIGURE 10. NOISE FLOOR FOR GAIN AND PHASE FAMILY OF CURVES VS FREQUENCY

### Typical Performance Characteristics (UHF-Band) (Continued)

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and PIN < -48dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .



SUPPLY CURRENT vs TEMPERATURE AT 770MHz 11.0  $HG V_{DD} =$ 10.5 HG V<sub>DD</sub> = 1.0 9.5  $HG V_{DD} = 1.8V$ (mA) 9.0  $LG V_{DD} = 1.7V$ 8.5 8.0  $LG V_{DD} = 1.9V$ 7.5 7.0 LG V<sub>DD</sub> = 1.8V 6.5 6.0 -40 85 -5 **TEMPERATURE (°C)** 

FIGURE 11. 3D NOISE FLOOR PLOT FOR GAIN AND PHASE FAMILY OF CURVES @ 750MHz

FIGURE 12. SUPPLY CURRENT VARIATION UNDER ECC

### **Typical Performance Characteristics (L-Band)**

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and  $P_{IN} < -48dBm$ , unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

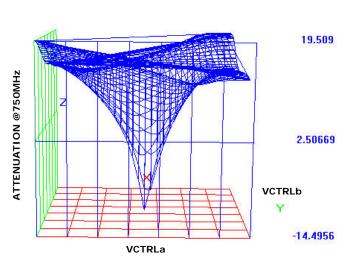


FIGURE 13. 3D CONTOUR PLOT FOR GAIN AND PHASE FAMILY OF CURVES IN HIGH GAIN MODE

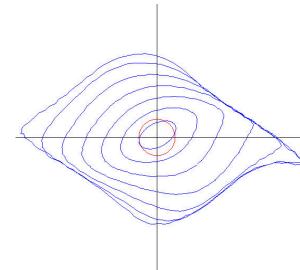


FIGURE 14. 2D CONTOUR PLOT FOR GAIN AND PHASE FAMILY OF CURVES IN HIGH BOOST MODE (RED CIRCLE = UNITY GAIN)

### Typical Performance Characteristics (L-Band) (Continued)

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and  $P_{IN} < -48dBm$ , unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

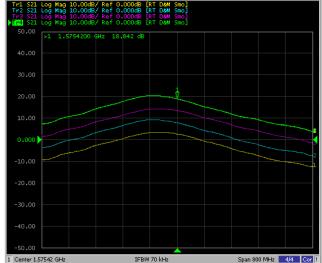


FIGURE 15. GAIN VS FREQUENCY AT LOW, MID, HIGH, AND BOOST GAIN SET POINTS

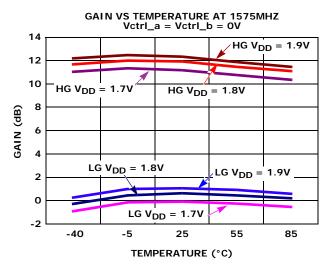


FIGURE 16. GAIN VARIATION UNDER ECC MEASURED
AT 1575MHz AT LOW GAIN AND HIGH GAIN
SET-POINTS

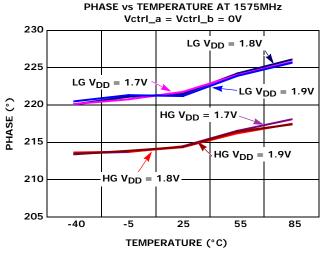


FIGURE 17. PHASE VARIATION UNDER ECC MEASURED
AT 1575MHz AT LOW GAIN AND HIGH GAIN
SET-POINTS

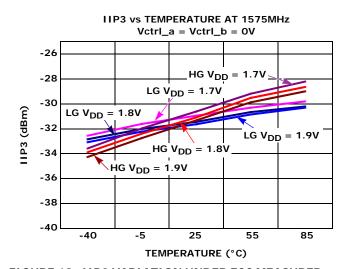


FIGURE 18. IIP3 VARIATION UNDER ECC MEASURED AT 1575MHz AT LOW GAIN AND HIGH GAIN SET-POINTS

### Typical Performance Characteristics (L-Band) (Continued)

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and  $P_{IN} < -48dBm$ , unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V \text{ to } 1.9V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}.$ 

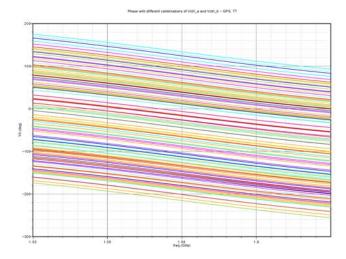
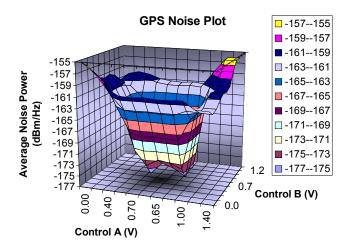


FIGURE 19. PHASE COVERAGE FOR GAIN AND PHASE **FAMILY OF CURVES vs FREQUENCY** 

FIGURE 20. NOISE FLOOR FOR GAIN AND PHASE **FAMILY OF CURVES vs FREQUENCY** 

SUPPLY CURRENT vs TEMPERATURE AT 1575MHz



 $+HG V_{DD} = 1.7V$ 10.0 HG V<sub>DD</sub> = 9.5 HG V<sub>DD</sub> = 9.0 DD (mA)  $LG V_{DD} = 1.9V$ 8.5 8.0  $LG V_{DD} = 1.7V$ 7.5 7.0 LG V<sub>DD</sub> = 1.8V 6.5 6.0 -40 -5 55

11.0

10.5

FIGURE 21. 3D NOISE FLOOR PLOT FOR GAIN AND PHASE FAMILY OF CURVES @ 1575MHz

FIGURE 22. SUPPLY CURRENT VARIATION UNDER ECC

TEMPERATURE (°C)

85

### Typical Performance Characteristics (ISM Band)

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and PIN < -48dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V$  to 1.9V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

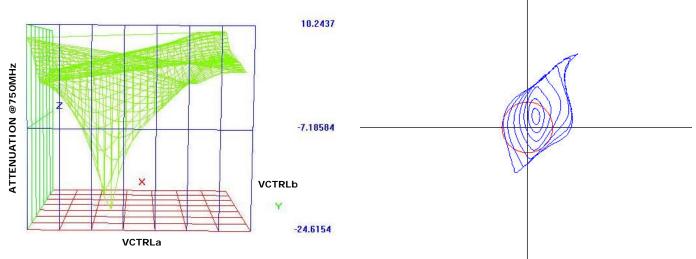


FIGURE 23. 3D ATTENUATION PLOT FOR GAIN AND PHASE FAMILY OF CURVES vs FREQUENCY

FIGURE 24. 2D CONTOUR PLOT FOR GAIN AND PHASE FAMILY OF CURVES IN BOOST MODE (RED CIRCLE = UNITY GAIN)

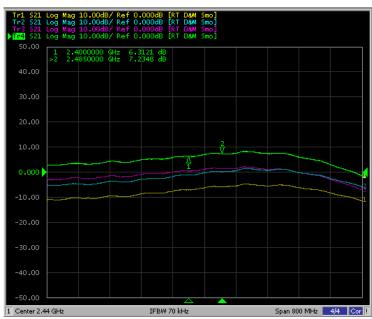
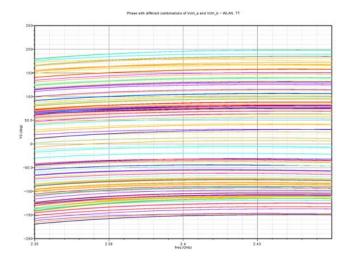


FIGURE 25. GAIN VS FREQUENCY AT LOW, MID, HIGH, AND BOOST GAIN SET POINTS

### Typical Performance Characteristics (ISM Band) (Continued)

Plots are exemplary only, to show typical performance and provide a frame of reference. Typical test conditions (TTC)  $V_{DD} = 1.8V$ ,  $T_A = +25^{\circ}C$ , and PIN < -48dBm, unless otherwise noted. Extreme Characterization Conditions (ECC) are  $V_{DD} = 1.7V \text{ to } 1.9V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}.$ 



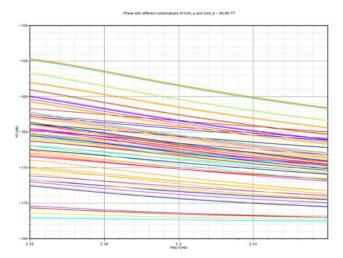


FIGURE 26. PHASE COVERAGE FOR GAIN AND PHASE **FAMILY OF CURVES** 

FIGURE 27. NOISE FLOOR FOR GAIN AND PHASE **FAMILY OF CURVES vs FREQUENCY** 

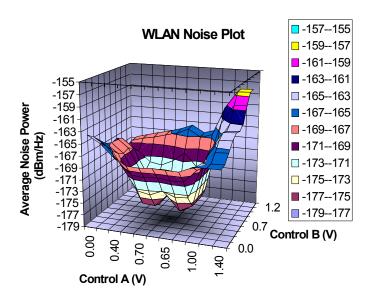


FIGURE 28. 3D NOISE FLOOR PLOT FOR GAIN AND PHASE FAMILY OF CURVES @ 2.4GHz

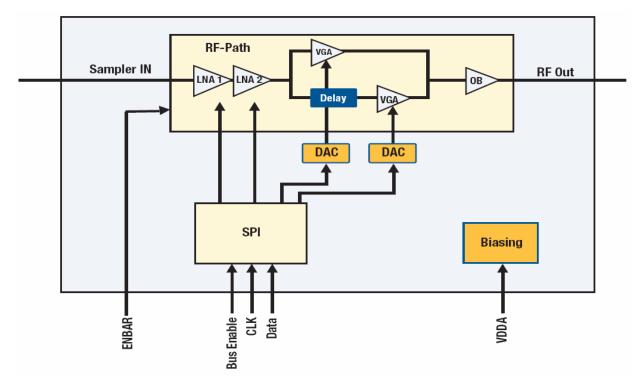


FIGURE 29. BLOCK DIAGRAM

### Operation

The architecture of the QHx220 is similar to that of a linear vector modulator. A SPI bus interface is used to control the internal 10-bit DACs, which in turn control the VGAs in the RF-path. The VGA settings sett the I and Q of a vector modulator and provide full control over the magnitude and phase of the output cancellation signal. The SPI interface is also used to control internal LNA gain stages at the sampler input, which can provide additional gain when sampling weaker noise sources. The QHx220 allows for a full 360° phase control and up to 50 dB of dynamic range of the input RF signal. This tuning range is used to emulate the RF noise coupling channel that is present between the noise source and victim receiver. The noise coupling channel can be radiated from the noise source to the victim receive antenna or via some other leakage path to the receiver - most often it is a combination of the two.

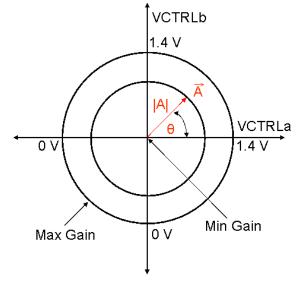


FIGURE 30. POLAR PLOT

Figure 30 illustrates the gain and phase control provided by the vector modulator. The coverage map is represented in polar form.

In practice it is not possible to reach origin at the minimum gain setting, which represents a gain of zero. This is due to the isolation limitations that exist in any device. Thus it is not possible to completely eliminate that signal in the forward path, resulting in minimum gain levels in the order of -45dBm or -55dBm.

#### **Evaluation Board**

General purpose evaluations boards are available for the QHx220 devices. They allow for basic functional testing of the IC. However, more importantly they are designed to be easily integrated into customer applications as an RF daughter card for initial proof of concept. The QHx220 has internal pre-amplification gain stages that can be used to amplify the sampled noise signal if additional gain is required to emulate the noise coupling channel. There are also internal DACs to control the amplitude and phase (I and Q) of the device. A software control GUI is provided to enable control of the device.

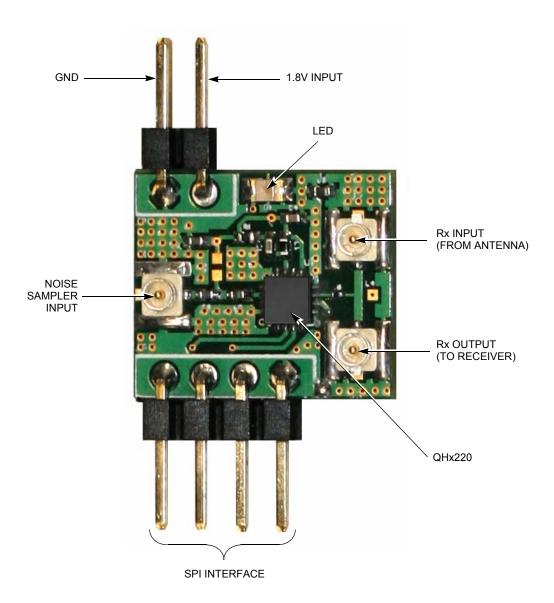


FIGURE 31. EVALUATION BOARD

#### Software GUI

A software interface is provided to facilitate the control of the evaluation board. The GUI can be used to control of the internal gain stages and DACs via a SPI bus interface. These two control signals are also referenced to as "I" (in phase") and "Q" (quadrature phase) control in the user interface. The QHx220 controller software is an application that uses the USB port of a PC to emulate the SPI bus communications to device. The initial user interface will look like the following:

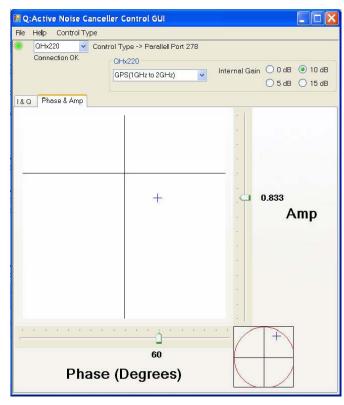


FIGURE 32. SOFTWARE GUI

The left tab within the window allows the user to directly set or sweep the I and Q values that control the QHx220. The right tab allows the user to control the Phase & Amplitude (which is simply a mathematical conversion of the I and Q values). Similarly to the I and Q panel, the Phase & Amplitude panel can be used to set or sweep the amplitude and phase of the QHx220 and is often a more intuitive approach to performing the optimization. In both cases a small window appears in the bottom right corner to illustrate the alternate I & Q or Phase and Amplitude representation.

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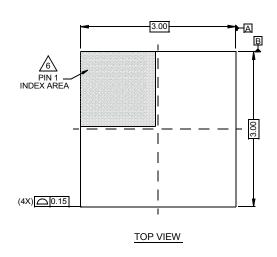
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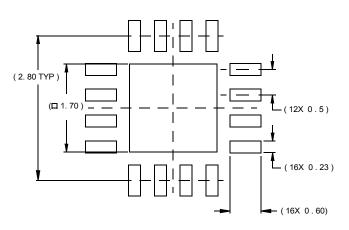
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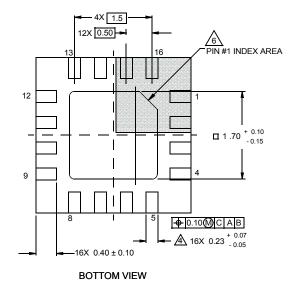
### **Package Outline Drawing**

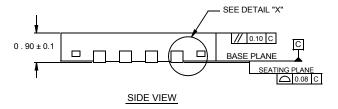
# L16.3x3B 16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE Rev 1, 4/07

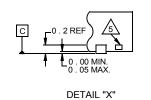




TYPICAL RECOMMENDED LAND PATTERN







#### NOTES:

- Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
- 2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
- 3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
- 4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- 5. Tiebar shown (if present) is a non-functional feature.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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