COMPARE LITE, STANDARD, AND PRO EDITIONS

Intel® Quartus® Prime Design Software

The Intel® Quartus® Prime software is number one in performance and productivity for FPGA, CPLD, and SoC designs, providing the fastest path to convert your concept into reality. The Quartus Prime software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

QUARTUS PRIME SOFTWARE DESIGN FLOW

	QUARTUS PRIME SOFTWARE KEY FEATURES	AVAILABILITY		
		LITE EDITION (FREE)	STANDARD EDITION ($)	PRO EDITION ($)
Device Support	Cyclone®, MAX®, and Arria® II device support	✓[1]	✓	
	Arria and Stratix® device support		✓	
	Arria 10 device support		✓	✓
Design Entry	Multiprocessor support (faster compile time)		✓	✓
	IP Base Suite	Available for purchase	✓	✓
	Qsys	✓	✓	✓
	Qsys Pro			✓
	Rapid Recompile		✓[2]	✓
	BluePrint Platform Designer			✓
Functional Simulation	ModelSim*-Intel FPGA Starter Edition software	✓	✓	✓
	ModelSim-Intel FPGA Edition software	✓[3]	✓[3]	✓[3]
Synthesis	Industry-standard language for design portability			✓
Placement and Routing	Fitter (Place and Route)	✓	✓	
	Incremental Optimization			✓
	Hybrid Placer		✓[4]	✓
Design Flow	Partial Reconfiguration			✓
Timing and Power Verification	TimeQuest Static Timing Analyzer	✓	✓	✓
	PowerPlay Power Analyzer	✓	✓	✓
In-System Debug	SignalTap™ II Logic Analyzer	✓[5]	✓	✓
	Transceiver toolkit		✓	✓
	JNEye link analysis tool		✓	✓
Operating System (OS) Support	Windows*/Linux* 64 bit support	✓	✓	✓
Add-On Development Tools	Intel FPGA SDK for OpenCL™	✓[3]	✓[3]	✓[3]
	DSP Builder for Intel FPGAs	✓[3]	✓[3]	✓[3]
	Nios® II Embedded Design Suite	✓	✓	✓
	Intel SoC FPGA Embedded Design Suite	✓	✓	✓
Price		Free	Buy Fixed - $2,995 Float - $3,995	Buy Fixed - $3,995 Float - $4,995
Download		Download Now	Download Now	Download Now

Notes:
1. The only Arria II FPGA supported is the EP2AGX45 device.
2. Available for Stratix V, Arria V, and Cyclone V devices.
3. Requires an additional license.
4. Available for Arria 10, Stratix V, Arria V, and Cyclone V devices.
5. OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission by Khronos.

QUARTUS PRIME DESIGN SOFTWARE FEATURES SUMMARY

DESIGN FLOW METHODOLOGY	BluePrint Platform Designer	Platform designer tool that enables you to quickly create your I/O design using real time legality checks.
	Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
	Qsys or Qsys Pro	Automates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect based on a network-on-a-chip architecture.
	Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Intel and from Intel's third-party IP partners.
	Synthesis	Now with expanded language support for System Verilog and VHDL 2008.
	Scripting support	Supports command-line operation and Tcl scripting, as well as graphical user interface (GUI) design.
	Rapid Recompile	Maximizes your productivity by reducing your compilation time up to 4X (for a small design change after a full compile). Improves design timing preservation.
	Incremental Optimization	The incremental optimizations capability in the Quartus Prime Pro Edition software offers a faster methodology to converge to design sign-off. The traditional fitter stage is divided into finer stages for more control over the design flow.
	Partial Reconfiguration	Create a physical region on the FPGA that can be reconfigured to execute different functions. Synthesize, place, route, close timing, and generate configuration bit streams for the functions implemented in the region.
PERFORMANCE AND TIMING CLOSURE METHODOLOGY	Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
	Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Quartus Prime software settings to find optimal results.
	Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
	Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
	Chip planner	Reduces verification time while maintaining timing closure by enabling small, post placement and routing design changes to be implemented in minutes.
VERIFICATION	TimeQuest timing analyzer	Provides native Synopsys Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
	SignalTap II logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
	System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
	PowerPlay technology	Enables you to analyze and optimize both dynamic and static power consumption accurately.
THIRD-PARTY SUPPORT	EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit www.altera.com/eda-partners.

Getting Started Steps

Step 1: Download the free Quartus Prime Lite Edition software

www.altera.com/download

Step 2: Get oriented with the Quartus Prime software interactive tutorial

After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training

www.altera.com/training

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