MC100LVEL90

-3.3V / -5V Triple ECL Input to LVPECL Output Translator

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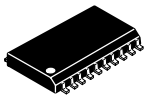


SO−20 WB
DW SUFFIX
CASE 751D

Description

The MC100LVEL90 is a triple ECL to LVPECL translator. The device receives either −3.3 V or −5 V differential ECL signals, determined by the V_{EE} supply level, and translates them to +3.3 V differential LVPECL output signals.

To accomplish the level translation, the LVEL90 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins, as expected, are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{EE}/2$ and the D input will be pulled to V_{EE}. This condition will force the Q output to a LOW, ensuring stability.

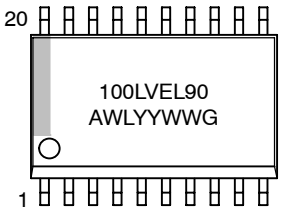
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- 500 ps Propagation Delays
- ESD Protection: >2 kV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC} = 3.0 V to 3.8 V;
  V_{EE} = −3.0 V to −5.5 V; GND = 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity;
  Pb Pkg Level 1,
  Pb−Free Pkg Level 3
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in,
  Oxygen Index: 28 to 34
- Transistor Count = 261 devices
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM*

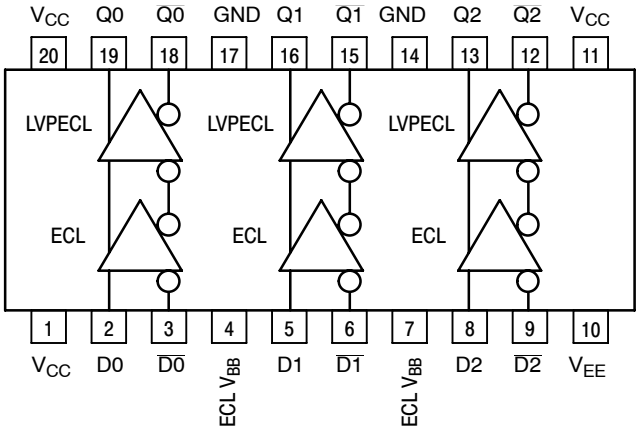


A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	ECL Inputs
Qn, $\overline{Qn}$	LVPECL Outputs
ECL V_{BB}	ECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

Figure 1. Logic Diagram and Pinout: 20-Lead SOIC (Top View)

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		−8 to 0	V
V_I	NECL Mode Input Voltage	GND = 0 V	$V_I \geq V_{EE}$	−6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	ECL V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. NECL INPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= −3.3 V; GND= 0 V (Note 1)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current			8.0		6.0	8.0			8.0	mA
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
ECL V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2)										
	Vpp < 500 mV	V_{EE}+1.3		−0.4	V_{EE}+1.2		−0.4	V_{EE}+1.2		−0.4	V
	Vpp ≧ 500 mV	VEE+1.5		−0.4	VEE+1.4		−0.4	VEE+1.4		−0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D	0.5			0.5			0.5			μA
	$\overline{D}$	−600			−600			−600			

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input parameters vary 1:1 with GND. V_{EE} can vary −3.0 V to −5.5 V.
2. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with GND.

Table 4. LVPECL OUTPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= −3.3 V; GND= 0 V (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			24		20	24			26	mA
V_{OH}	Output HIGH Voltage (Note 4)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 4)	1470	1605	1745	1490	1600	1680	1490	1595	1680	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.5 V / −0.3 V. V_{EE} can vary −3.0 V to −5.5 V.
4. Outputs are terminated through a 50 Ω resistor to V_{CC}−2 volts.

Table 5. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.8 V; V_{EE}= −3.0 V to −5.5 V; GND = 0 V

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
fmax	Maximum Toggle Frequency		560			650			700		MHz
t_{PLH} t_{PHL}	Propagation Delay Diff D to Q S.E.	390 340		590 640	420 370		620 670	460 410		660 710	ps
t_{SKEW}	Skew Output−to−Output (Note 5) Part−to−Part (Diff) (Note 5) Duty Cycle (Diff) (Note 6)		20 25	100 200 		20 25	100 200 		20 25	100 200 	ps
tJITTER	Random Clock Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Differential Configuration) (Note 7)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% − 80%)	230		500	230		500	230		500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Skews are valid across specified voltage range, part−to−part skew is for a given temperature.
6. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
7. V_{PP}(min) is swing measured single−ended on each input in differential configuration. The device has a DC gain of ≈40.

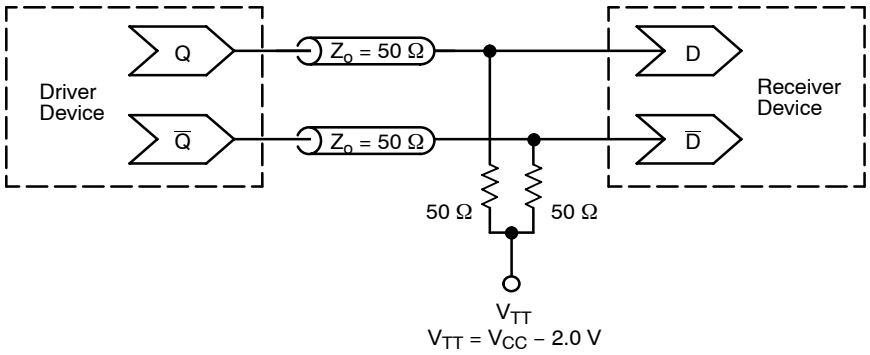


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Package†
MC100LVEL90DW	SOIC−20	38 Units / Rail
MC100LVEL90DWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC100LVEL90DWR2	SOIC−20	1000 / Tape & Reel
MC100LVEL90DWR2G	SOIC−20 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

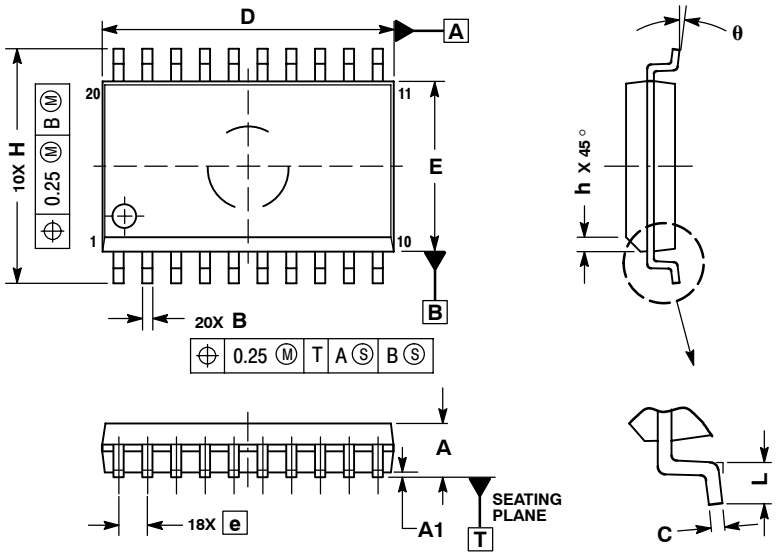
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SO−20 WB
DW SUFFIX
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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