Active AT85C51SND3Bx Errata List

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AT85C51SND3Bx Errata History

Lot Number	Errata List
All	1, 2, 3, 4, 5, 6

AT85C51SND3Bx Errata Description

1. I/O Ports – P0, P2, P4, P5 Read-Modify-Write

The P0, P2, P4, P5 implementation may lead to Input lock-up when using read-modify-write (RMW) instructions:

ANL	(logical AND, e.g., ANL P2,A)
ORL	(logical OR, e.g., ORL P2,A)
XRL	(logical EX-OR, e.g., XRL P2,A)
JBC	(jump if bit set and clear bit, e.g., JBC P2.1, LABEL)
CPL	(complement bit, e.g., CPL P2.0)
INC	(increment, e.g., INC P2)
DEC	(decrement, e.g., DEC P2)
DJNZ	(decrement and jump if not zero, e.g., DJNZ P2, LABEL)
MOV PX.Y,C	(move carry bit to bit Y of Port X)
CLR PX.Y	(clear bit Y of Port X)
SETB PX.Y	(set bit Y of Port X)

Here is a normal I/O port RMW execution sequence:

– Read the I/O port SFR (latch)

– Modify the data

– Write back the modified data to port SFR

Now here is what is really executed, these instructions that should read the internal latch read in fact the port data:

– Read the I/O port data

– Modify the data

– Write back the modified data to port SFR

Here is a detailed example:
P0.0 is used as input (set low by external hardware) while other P0 I/O are used as output.
Following code may set P0.1 and leave other bits unaffected:

```
setb P0.1;
```

– before executing, P0 SFR= 1111 1101; P0 port= 1111 1100

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– after executing, P0 SFR= 1111 1110; P0 port= 1111 1110
Now P0.0 is no more programmed as input. The latch content is set to 0 meaning the port is internally driven to low level like for an output.

Workaround

To avoid any conflict with port inputs, put all application inputs on same port. If this is not possible, avoid using RMW instructions and rebuild such instruction by software by taking care to set the Port SFR bit to 1 when writing back to SFR.

2. SIO Interface – Low Baudrate Data Reception Ready Report

RI flag reset time too long after reading data into the reception FIFO. This may report bad data reception and lead to double read of received characters.
This errata depends on the CPU frequency and the treatment done on the received character, it appears using polling mode and using low baudrate values.

Workaround

The goal of the workaround is to leave enough time to the RI flag to be reset to forbid a bad reception (RI=1) detection. Two workaround are proposed:

– Limit the baudrate to high values, e.g. > 50Kbaud with Fosc= 12MHz, X2 mode and 12x oversampling factor.
– Add a delay between two reads of a character.

3. SPI Interface – DFC Usage Limitation

DFC transfers to SPI do not operate properly when DFC is clocked by PLL.

Workaround

Use DFC transfer only with DFC clocked by oscillator.

4. Battery Monitor – Bad Conversion Linearity

Battery monitor reports bad linearity data.

Workaround

Use the VB4:0 value as threshold voltage conversion only, do not use it for full range voltage conversion.

5. ISP – ISP Entry When Blanked Nand Flash

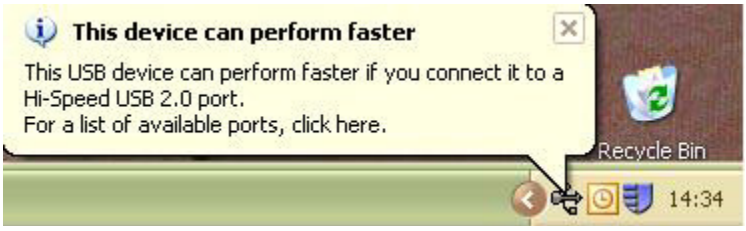
The ISP mode is not automatically started when first powered-up with new blanked Nand Flash. This case specially appears when in production.

Workaround

Use a key of the keyboard matrix to force ISP entry at power-up. This is achieved by connecting any column signal to ISP pin. Then pressing the key connected to this column and to ROW 0 will assert the ISP pin.
Note that this workaround forbids debug mode as $\overline{\text{ISP}}$ pin is also the OCDT pin. Solution is to add a 0 Ω resistor in order to insulate the OCDT pin from the keypad during debugging.
For an example on how to apply the workaround, refer to the at85rfd-07 schematic.

6. ISP – ISP USB enumeration on Windows™ XP

When connecting the device to windows XP, an informational pop-up is opened near the status bar:



This is a windows dummy message since ISP is done in full speed mode.

Workaround

None. Do not take care of this pop-up.

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