



# PSMN2R8-25MLC

N-channel 25 V 2.8 mΩ logic level MOSFET in LFAK33 using NextPower Technology

Rev. 3 — 15 June 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

### 1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

### 1.4 Quick reference data

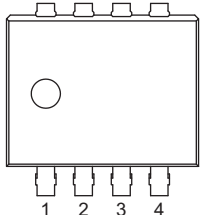
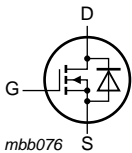
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	[1]	-	70	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	88	W
$T_j$	junction temperature		-55	-	175	$^\circ\text{C}$
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 10</a>	-	3.25	3.75	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 10</a>	-	2.45	2.8	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 12.5\text{ V}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	3.9	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 12.5\text{ V}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	16.3	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT1210 (LFAK33)

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN2R8-25MLC	LFAK33	Plastic single ended surface mounted package (LFAK33); 4 leads	SOT1210

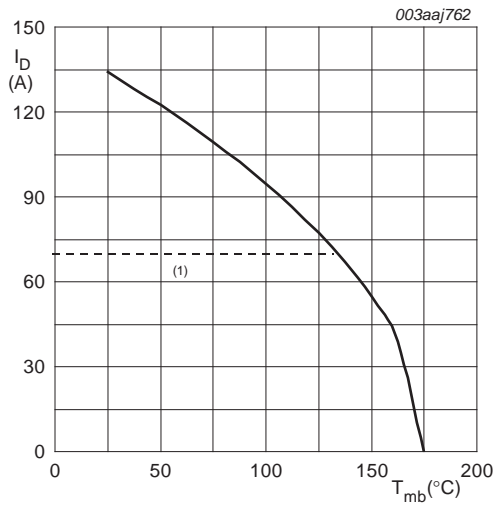
## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

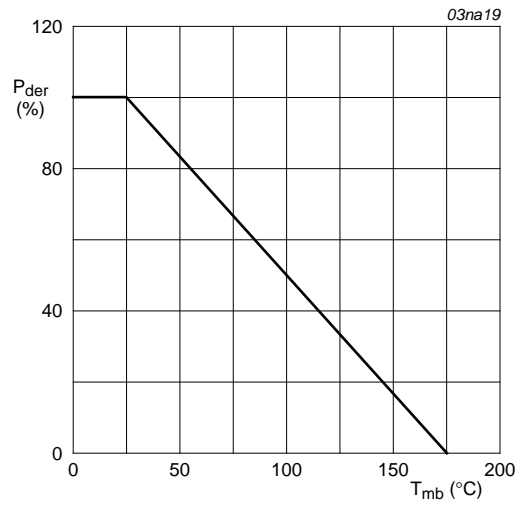
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	25	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	70	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	70	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 4</a>	-	536	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	88	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
$V_{ESD}$	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	350	-	V
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	70	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	536	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 70\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; see <a href="#">Figure 3</a>	-	77	mJ

[1] Continuous current is limited by package.



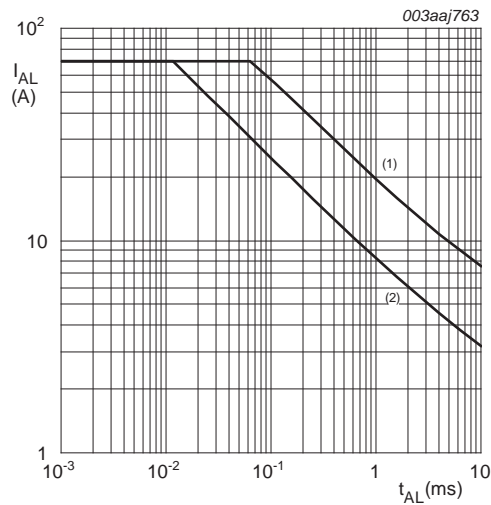
$V_{GS} \geq 10V$   
 (1) Capped at 70 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{Tot}}{P_{Tot(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



(1)  $T_{j(jmb)} = 25^{\circ}C$ ; (2)  $T_{j(jmb)} = 100^{\circ}C$

**Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time**

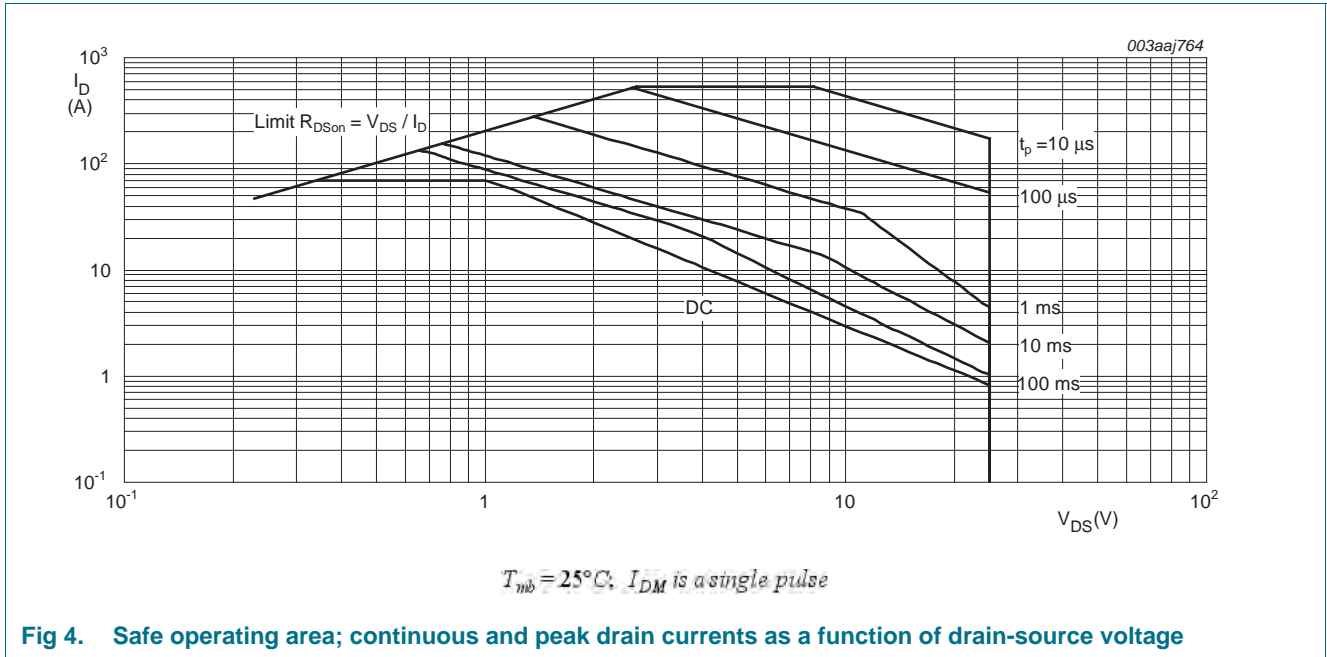


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	1.49	1.7	K/W

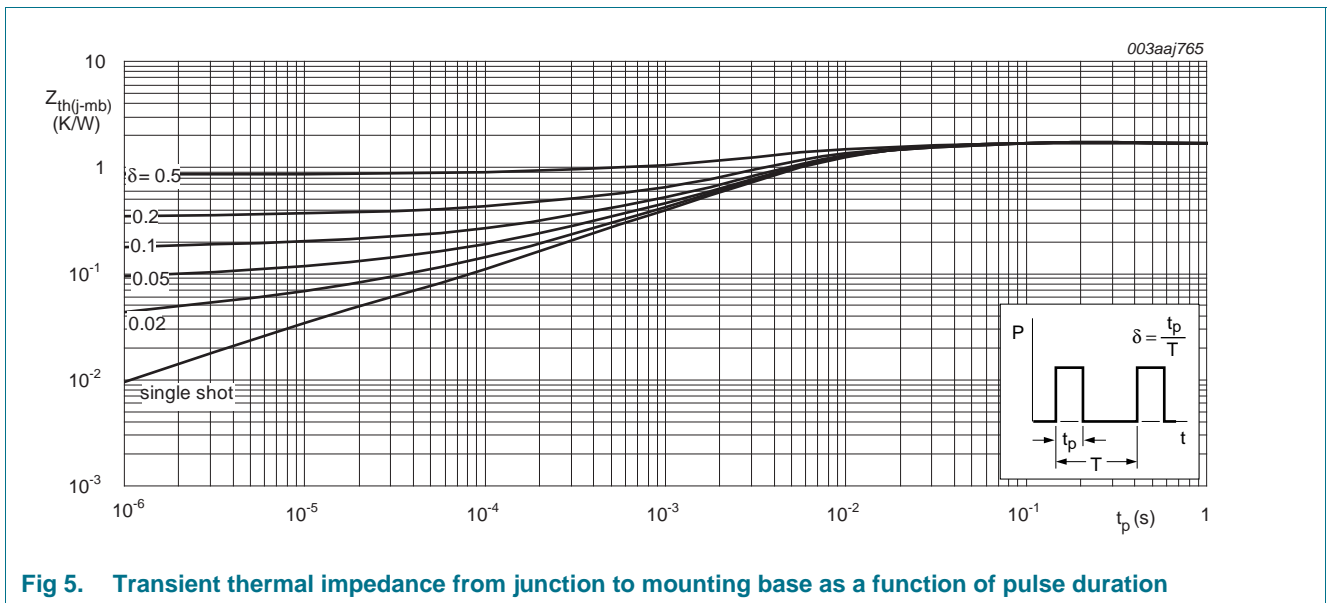


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

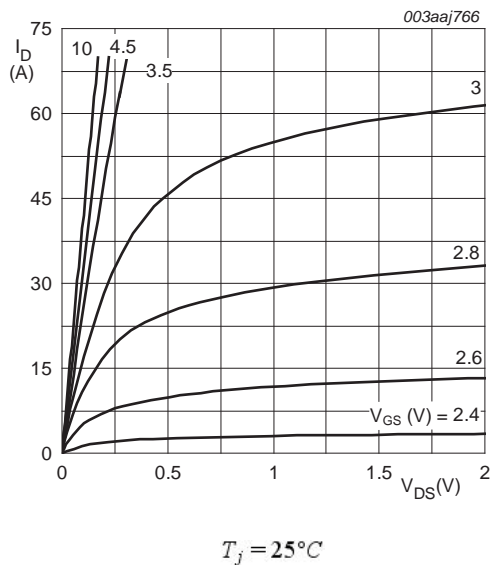
## 6. Characteristics

**Table 6. Characteristics**

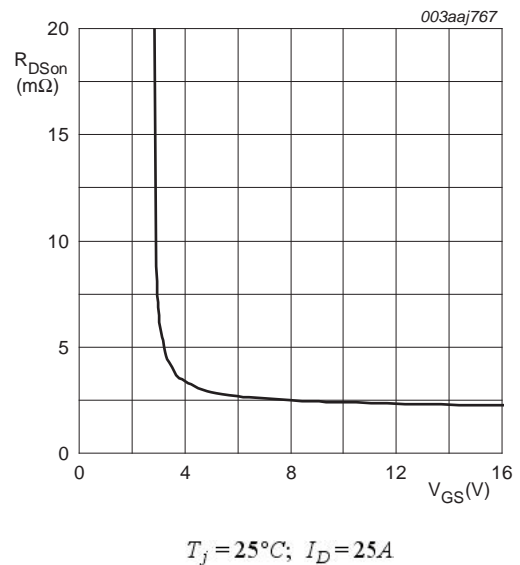
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1.45	1.74	2.15	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-4.2	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	3.25	3.75	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	-	6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	2.45	2.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	-	4.5	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	0.37	0.74	1.48	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12.5 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	37.7	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 12.5 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	16.3	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	36.7	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12.5 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	6.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	3.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.6	-	nC
$Q_{GD}$	gate-drain charge		-	3.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 12.5 \text{ V};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	2.9	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12.5 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	2432	-	pF
$C_{oss}$	output capacitance		-	533	-	pF
$C_{rss}$	reverse transfer capacitance		-	198	-	pF

**Table 6. Characteristics ...continued**

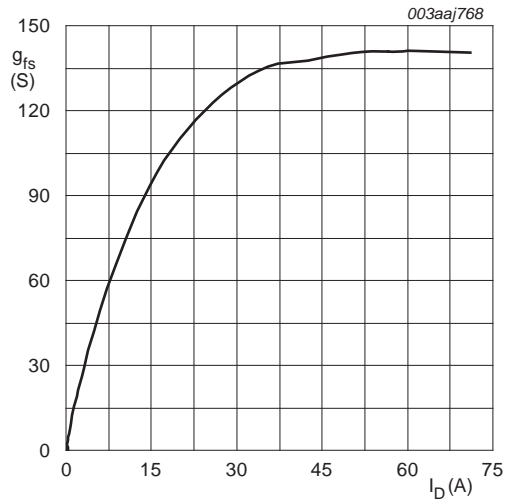
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12.5\text{ V}; R_L = 0.5\ \Omega; V_{GS} = 4.5\text{ V};$	-	16.4	-	ns
$t_r$	rise time	$R_{G(ext)} = 5\ \Omega$	-	24.6	-	ns
$t_{d(off)}$	turn-off delay time		-	19.9	-	ns
$t_f$	fall time		-	13.1	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12.5\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	14.3	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	0.82	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	21.3	-	ns
$Q_r$	recovered charge	$V_{DS} = 12.5\text{ V}$	-	14.1	-	nC
$t_a$	reverse recovery rise time	$V_{GS} = 0\text{ V}; I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s};$ $V_{DS} = 12.5\text{ V};$ see <a href="#">Figure 16</a>	-	12.1	-	ns
$t_b$	reverse recovery fall time		-	9.2	-	ns



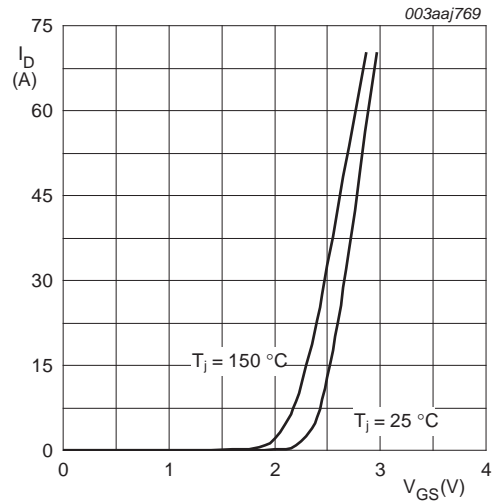
**Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



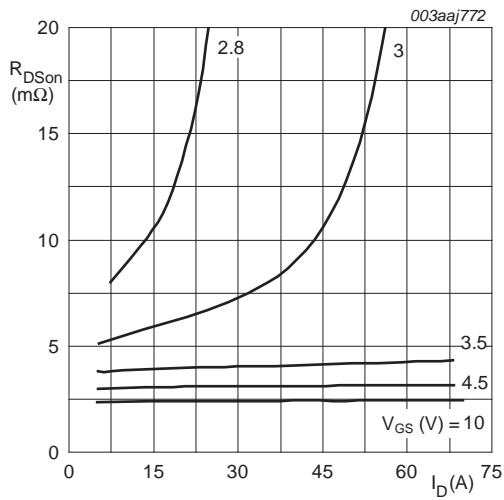
**Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



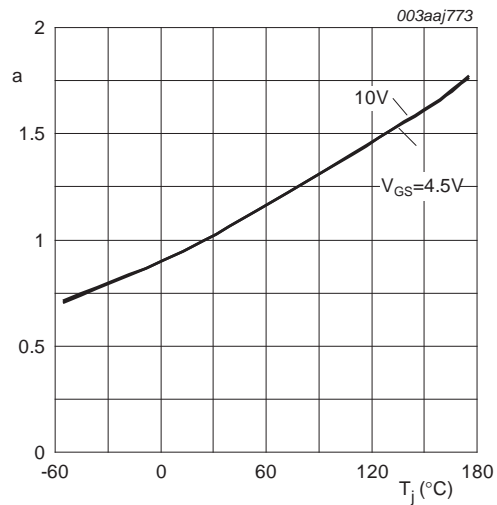
**Fig 8. Forward transconductance as a function of drain current; typical values**



**Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



**Fig 10. Drain-source on-state resistance as a function of drain current; typical values**



**Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

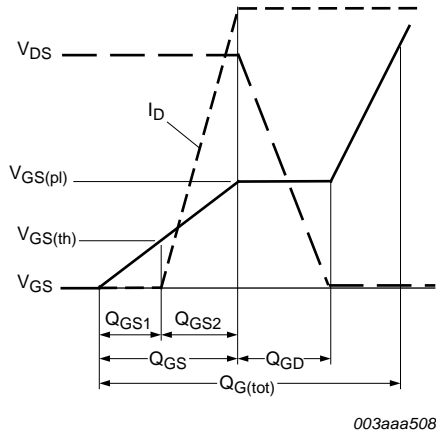
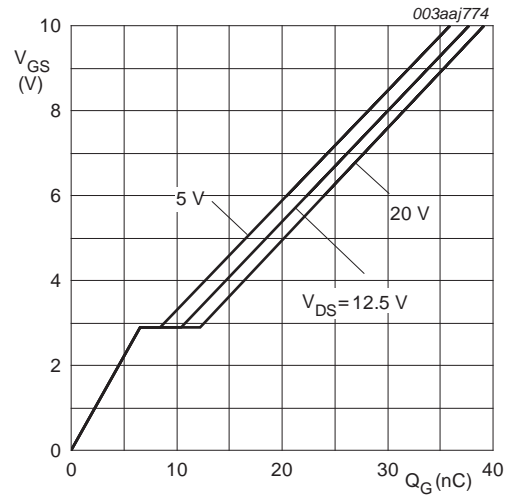
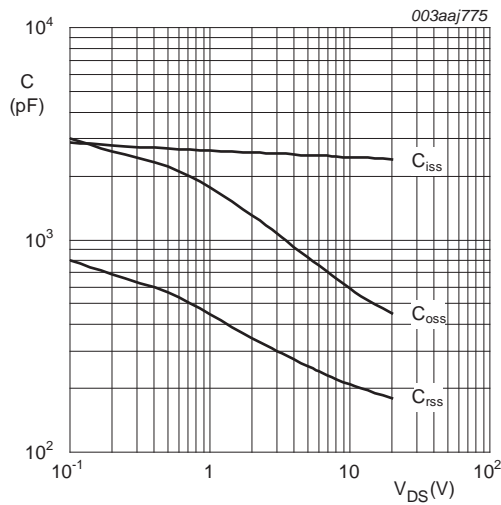


Fig 12. Gate charge waveform definitions



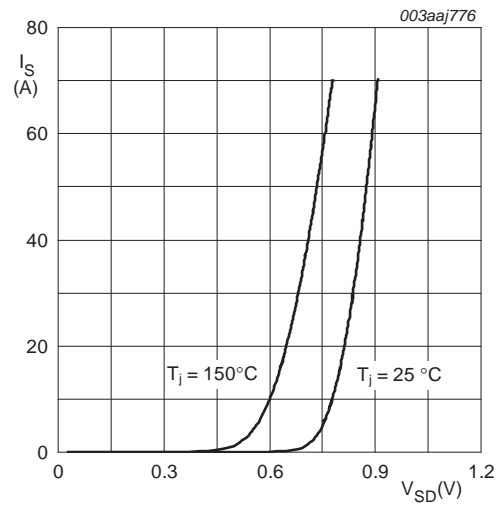
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{V}$

Fig 15. Source current as a function of source-drain voltage; typical values



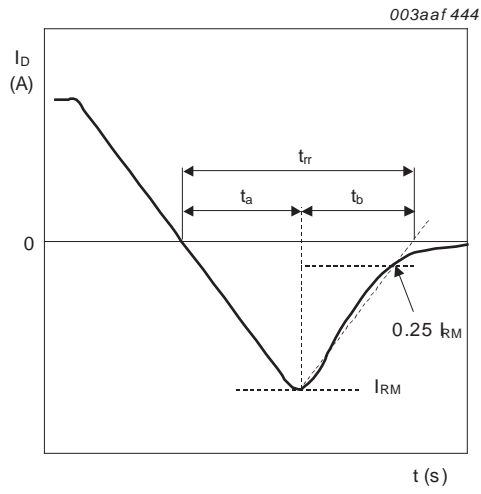


Fig 16. Reverse recovery timing definition

## 7. Package outline

Plastic single ended surface mounted package (LPAK33); 8 leads

SOT1210

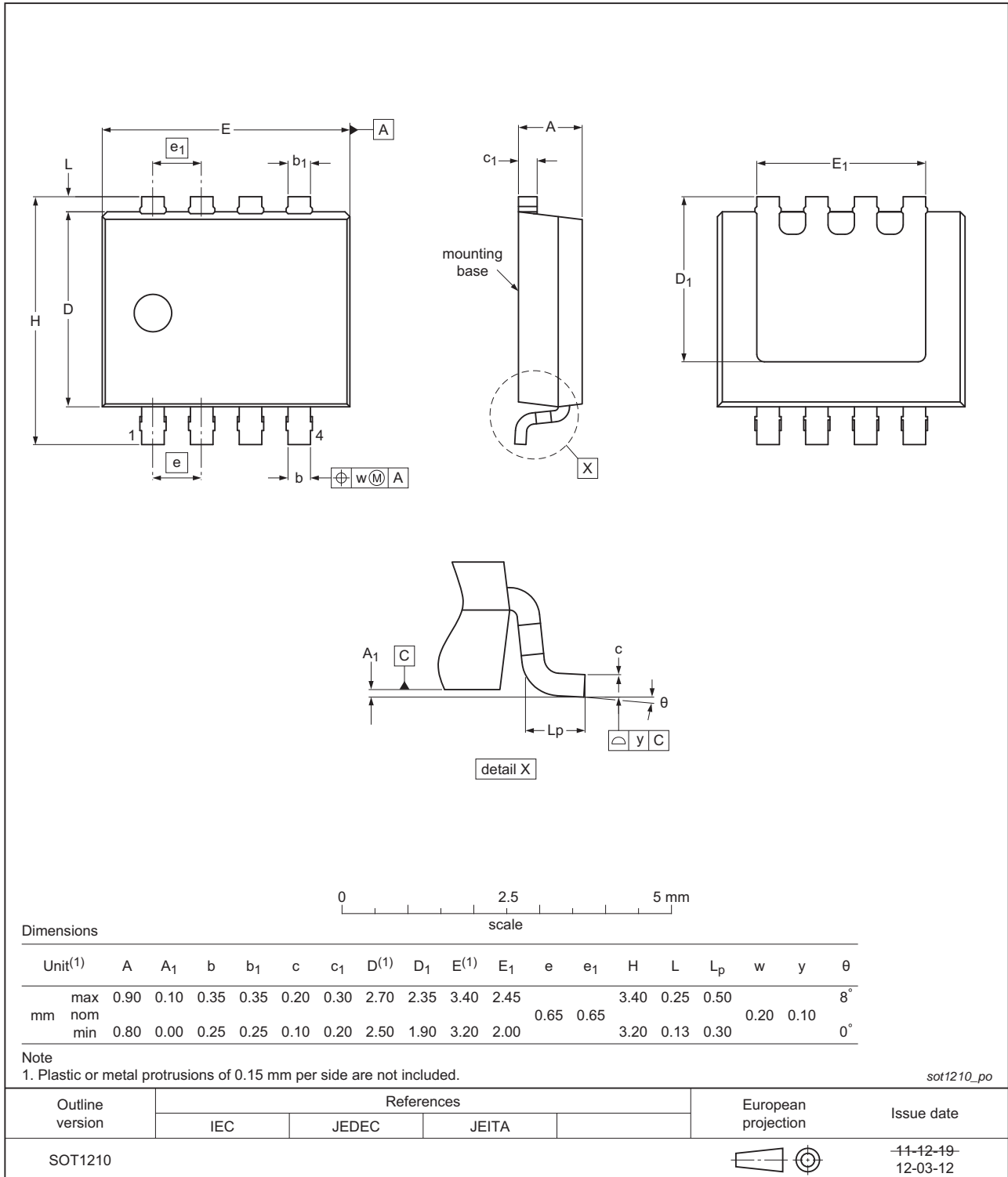


Fig 17. Package outline SOT1210 (LPAK33)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R8-25MLC v.3	20120615	Product data sheet	-	PSMN2R8-25MLC v.2
Modifications:	• Various changes to content.			
PSMN2R8-25MLC v.2	20120607	Product data sheet	-	PSMN2R8-25MLC v.1

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1]</sup> [2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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