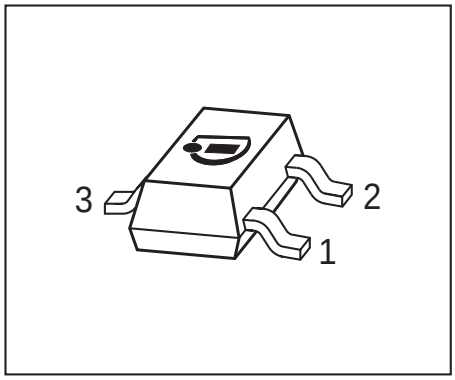
Silicon N-Channel MOSFET Triode



- For high-frequency stages up to 300 MHz preferably in FM applications
- Pb-free (RoHS compliant) package[1)]
- Qualified according AEC Q101

AEC Qualified RoHS

ESD (**E**lectro**s**tatic **d**ischarge) sensitive device, observe handling precaution!

Type	Marking	Pin Configuration						Package
BF999	LBs	1=G	2=D	3=S	-	-	-	SOT23

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	20	V
Continuous drain current	I_D	30	mA
Gate-source peak current	$\pm I_{GSM}$	10	mA
Total power dissipation $T_S \leq 76$ °C	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point[2)]	R_{thchs}	≤ 370	K/W

[1]Pb-containing package may be available upon special request
[2]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

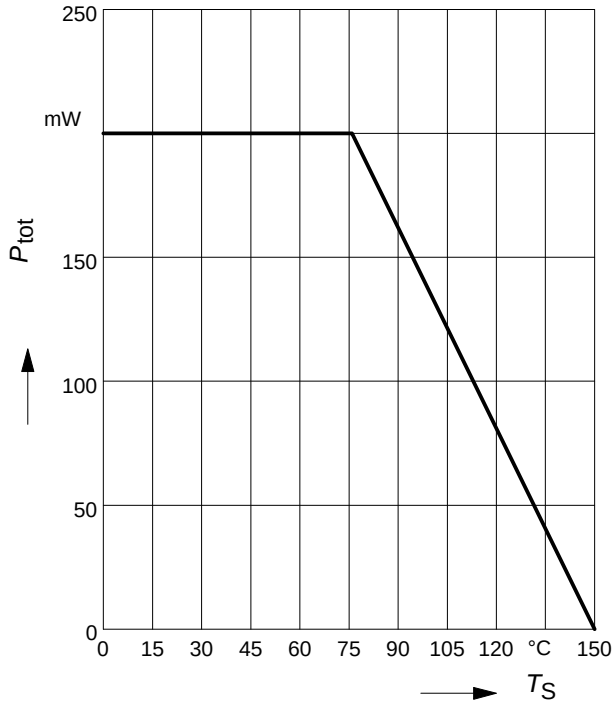
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 10 µA, -V_{GS} = 4 V	$V_{(BR)DS}$	20	-	-	V
Gate-source breakdown voltage ± I_{GS} = 10 mA, V_{DS} = 0	±$V_{(BR)GSS}$	6.5	-	12	
Gate-source leakage current ± V_{GS} = 5 V, V_{DS} = 0	± I_{GSS}	-	-	50	nA
Drain current V_{DS} = 10 V, V_{GS} = 0	I_{DSS}	5	10	16	mA
Gate-source pinch-off voltage V_{DS} = 10 V, I_D = 20 µA	-$V_{GS(p)}$	-	0.8	1.5	V

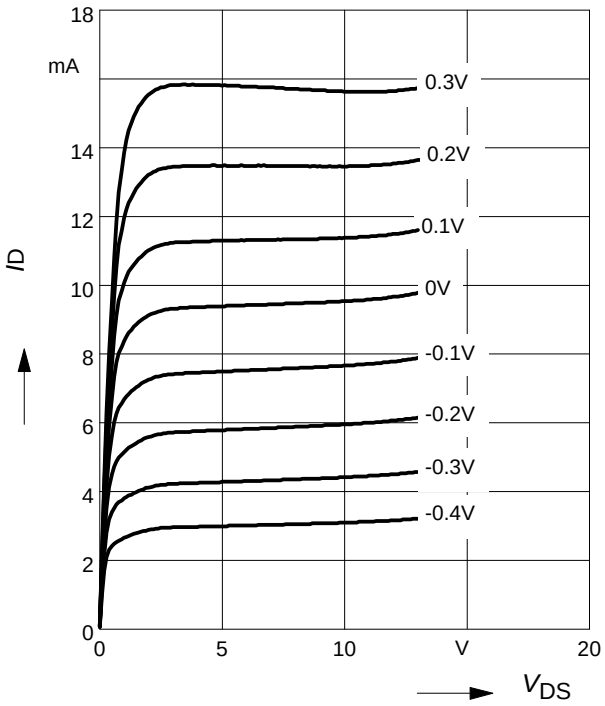
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Forward transconductance V_{DS} = 10 V, I_D = 10 mA	g_{fs}	14	20	-	mS
Gate input capacitance V_{DS} = 10 V, I_D = 10 mA, f = 10 MHz	C_{gss}	-	2.5	-	pF
Output capacitance V_{DS} = 10 V, I_D = 10 mA, f = 10 MHz	C_{dss}	-	0.9	-	pF
Power gain V_{DS} = 10 V, I_D = 10 mA, f = 45 MHz	G_p	-	27	-	dB
Noise figure V_{DS} = 10 V, I_D = 10 mA, f = 45 MHz	F	-	2.1	-	dB

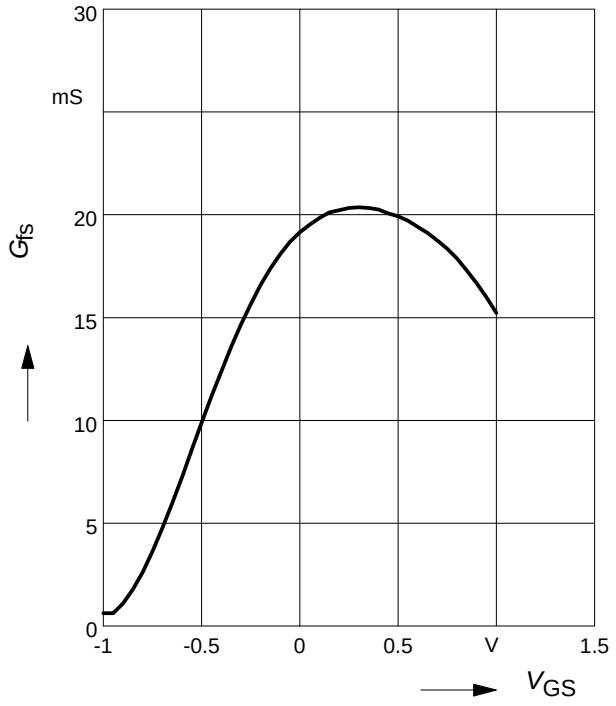
Total power dissipation $P_{tot} = f(T_S)$



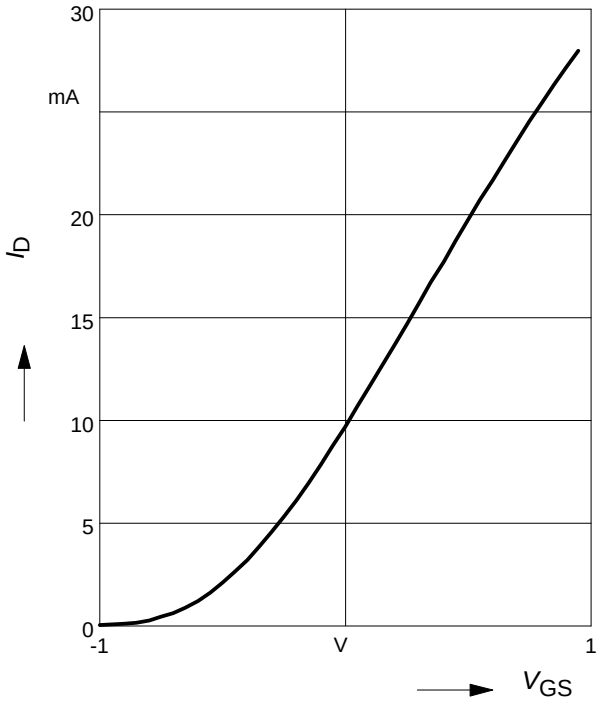
Output characteristics $I_D = f(V_{DS})$



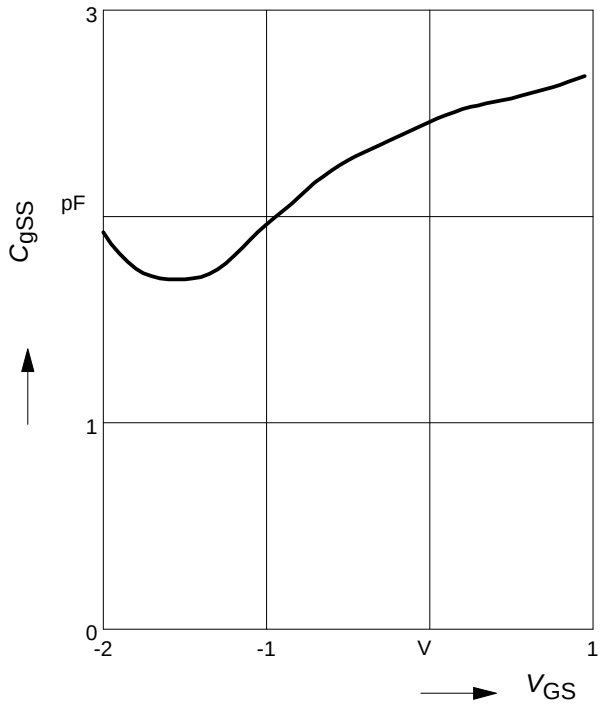
Gate transconductance $g_{fs} = f(V_{GS})$



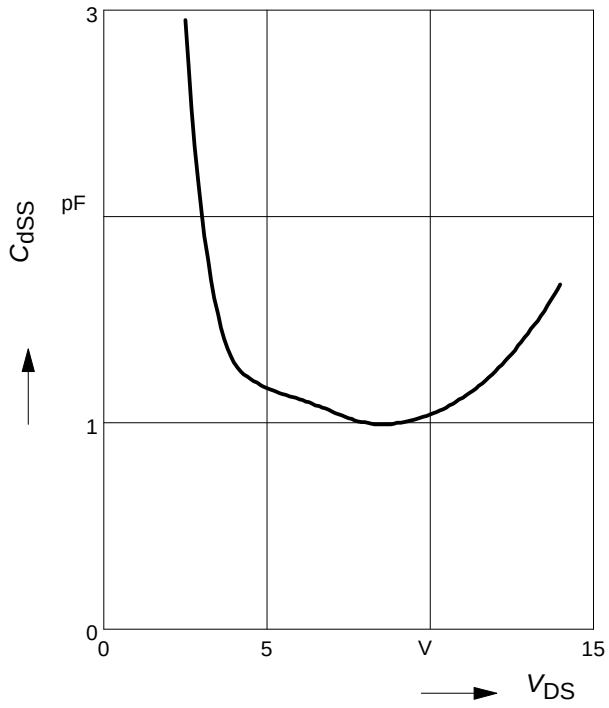
Drain current $I_D = (V_{GS})$



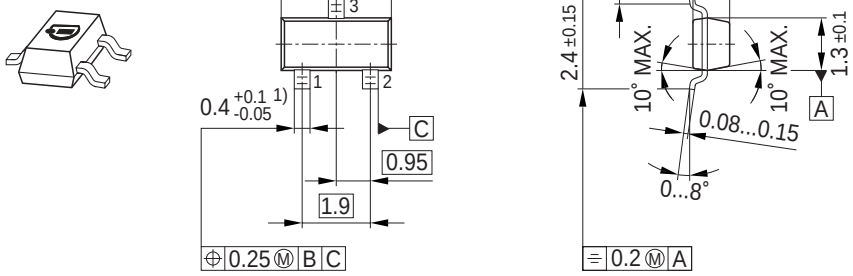
Gate input capacitance $C_{gss} = f(V_{GS})$



Output capacitance $C_{dss} = f(V_{DS})$

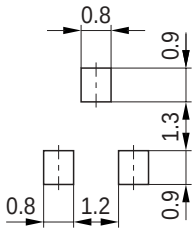


Package Outline

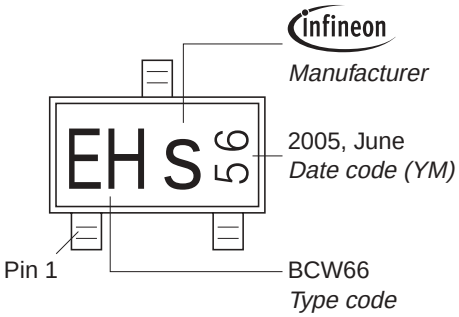


1) Lead width can be 0.6 max. in dambar area

Foot Print

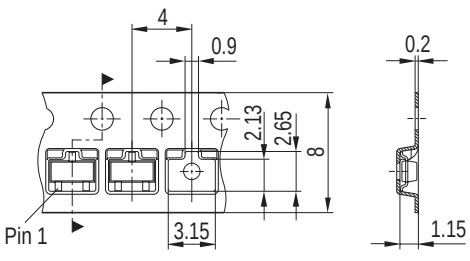


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



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