Preliminary

SG923-0007 Evaluation Kit

Overview

SG923-0007 Is an evaluation Kit used to simplify the rapid evaluation and software integration of the SG901-1071 Radio Module. The EVK allows for easy access to the SDIO interface via a standard SDIO hardware connector as well as a break out of each pin for debugging. The SDIO connector is designed to plug into processor development boards for rapid software testing.

The SG901-1080 Carrier board which hosts the SG901-1071 board also contains a debug connector which hosts the Blue Tooth coexistence control interface as well as a Debug SPI interface.

The evaluation kit can provide power to the module from a 3.3V SDIO socket or external input for instrumentation. A 2.4GHz antenna connection port as well as an optional external Bluetooth interface allow for complete system testing.

The Kit consists of a SG901-1071 soldered into a Carrier Board, Sagrad Part Number SG901-1080, Figure 1 and a SDIO/SPI Adapter Board, Sagrad Part number SG901-1042 depicted on Figure 2.

Most signals can also be used as general-purpose IO, and are available at standard 0.1" pitch headers for SPI applications and SDIO form factor for SDIO applications. An interface for external Bluetooth access is available in a 2mm pitch header.

Features

- Easy to connect to SPI and SDIO header
- Easy to use SDIO connector for common processor EVK.
- SDIO break out header for logic analysis and driver development
- Bluetooth test port and Coexistence testing header.
- Full application circuit example.
- Standard 3.3V Powered SDIO on Insert
- SPI and Supply Connector
- On board Regulator and Sleep Clock Oscillator
- Simple Client application
- Versatile SDIO and SPI Bus

Ordering Information

Packaging	Order Number
Evaluation Kit	SG923-0007

Software Support and Drivers

Updated versions of all software are available at: www.sagrad.com/support/1071

Full Assembly View

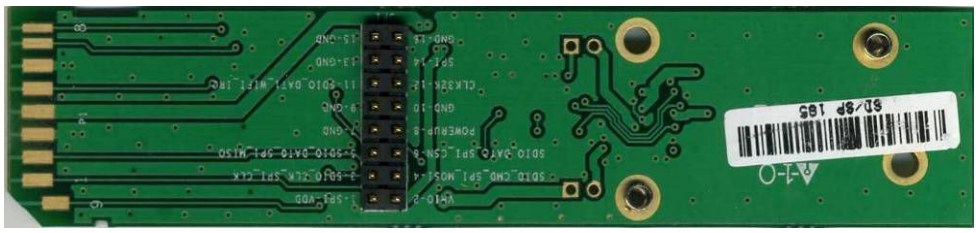
FIGURE 1: SG901-1080 Carrier Board
(Includes the SG901-1071 Module)

Top View

Bottom View

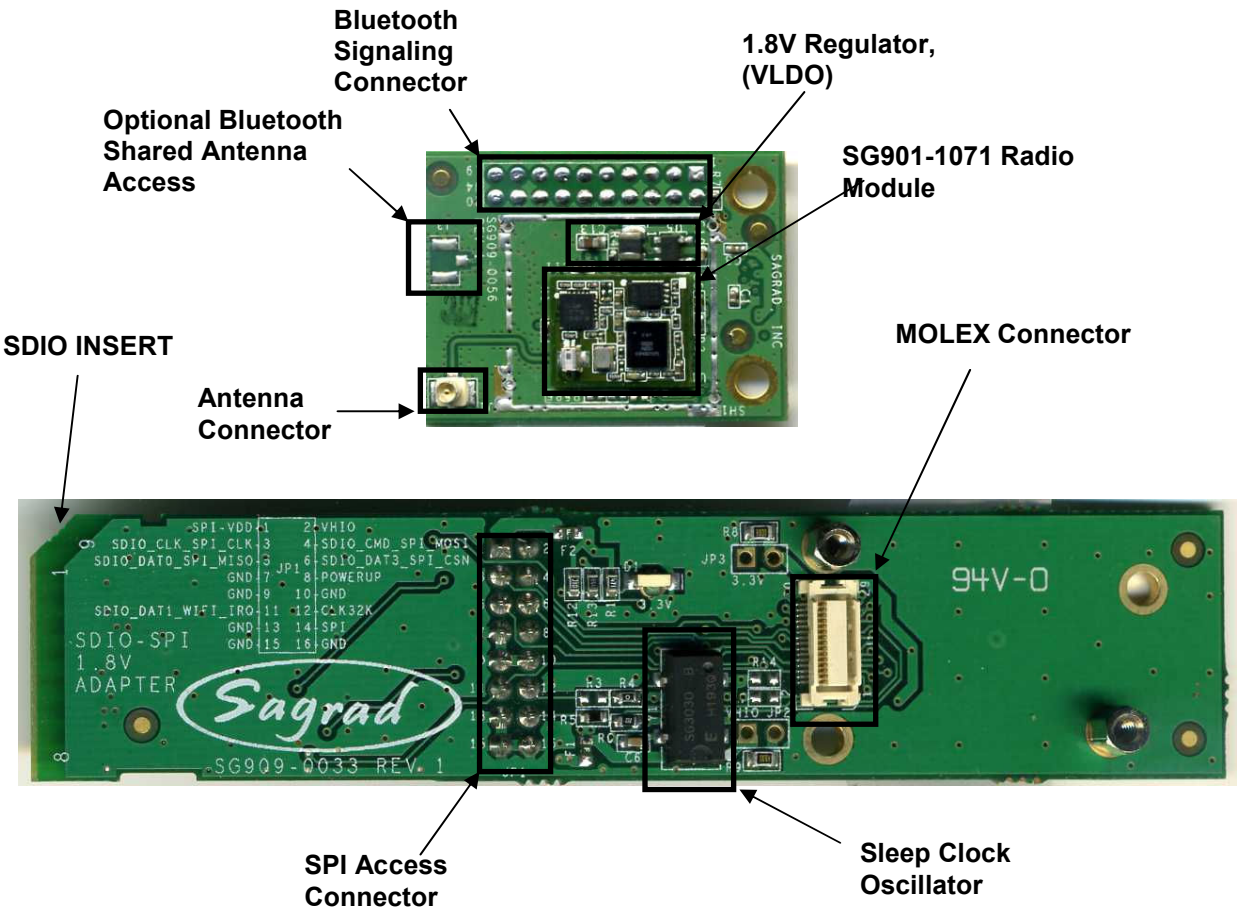
FIGURE 2: SG901-1042 Adapter Board

Top View



Bottom View

SG923-0007 Evaluation Kit Boards Main Components



Connector Descriptions

Some of the pin functions on the SG901-1071 are multiplexed between the SPI and SDIO applications. Note that the same Module pins may appear into both SDIO and SPI connectors.

The following tables explain the functionality per Bus application. The notes explain the mapping to the SG901-1071 Module pin nomenclature.

SDIO INSERT Pin Descriptions

SIGNAL NAME	PIN NUMBER	DESCRIPTION	NOTES
SDIO_DAT[3]	1	SDIO DATA3	Mapped to CS_SDD3 on SG901-1071 Module
SDIO_CMD	2	SDIO CMD	Mapped to SDCMD on SG901-1071 Module
VSS1	3	VSS, Ground Return	
VDD	4	SDIO_VDD	Mapped and connected to VHIO and 3.3V on the SG901-1071. (NOTE: Jumper between pins 1 and 2 of the JP1 connector on the adapter board)
CLK	5	SDIO Clock	Mapped to SDCLK on SG901-1071 Module
VSS2	6	VSS, Ground Return	
SDIO_DAT[0]	7	SDIO DATA0	Mapped to SDD3 on SG901-1071 Module
SDIO_DAT[1]	8	SDIO DATA1	Mapped to SDD1 on SG901-1071 Module
SDIO_DAT[2]	9	SDIO DATA2	Mapped to SDD2 on SG901-1071 Module
NOTE: Pin 9 of the standard SDIO pin out is recessed and collocated with pin 1			

SPI Pin Descriptions (JP1 on the adapter board schematics)

SIGNAL NAME	PIN NUMBER	DESCRIPTION	NOTES
SPI_VDD	1	VDD (external)	Mapped to 3.3V supply on SG901-1071 Module (Requires external power supply at 3.3V)
VHIO	2	VHIO	Mapped to VHIO input on SG901-1071 Module. (use a jumper to PIN 1 in case the VHIO is 3.3V or apply an external VHIO source if lower than 3.3V)
SPI_CLK	3	SPI Clock	(VHIO Domain) Mapped to SDCLK on SG901-1071 Module
SPI_MOSI	4	SPI Master out-Slave in	(VHIO Domain) Mapped to SDCMD on SG901-1071 Module
SPI_MISO	5	SPI Master in-Slave out	(VHIO Domain) Mapped to SDD0 on SG901-1071 Module
SPI_CSN	6	SPI Chip Select	(VHIO Domain) Mapped to SDD3 on SG901-1071 Module
GND	7	Ground Return	
POWERUP	8	Power Up WIFI	Mapped to POWERUP on SG901-1071 Module. This pin is normally high in the adapter board by an internal resistor divider to 3.3V. Use a low level input to disable the SG901-1071
GND	9	Ground Return	
GND	10	Ground Return	
WIFI_IRQ	11	Interrupt Request	(VHIO Domain) Mapped to SDD1 on SG901-1071 Module
CLK32K	12	Not used in this application	An on board Low frequency clock is connected to the SLEEPCLK on the SG901-1071
GND	13	Ground Return	
SPI	14	Not used in this application	
GND	15	Ground Return	
GND	16	Ground Return	

Bluetooth Signaling Pins (J4 on Carrier Board Schematics)

SIGNAL NAME	PIN NUMBER
WLAN_DENY	9
BT_ACTIVE	11
BT_PERIODIC	13
BT_STATUS	15

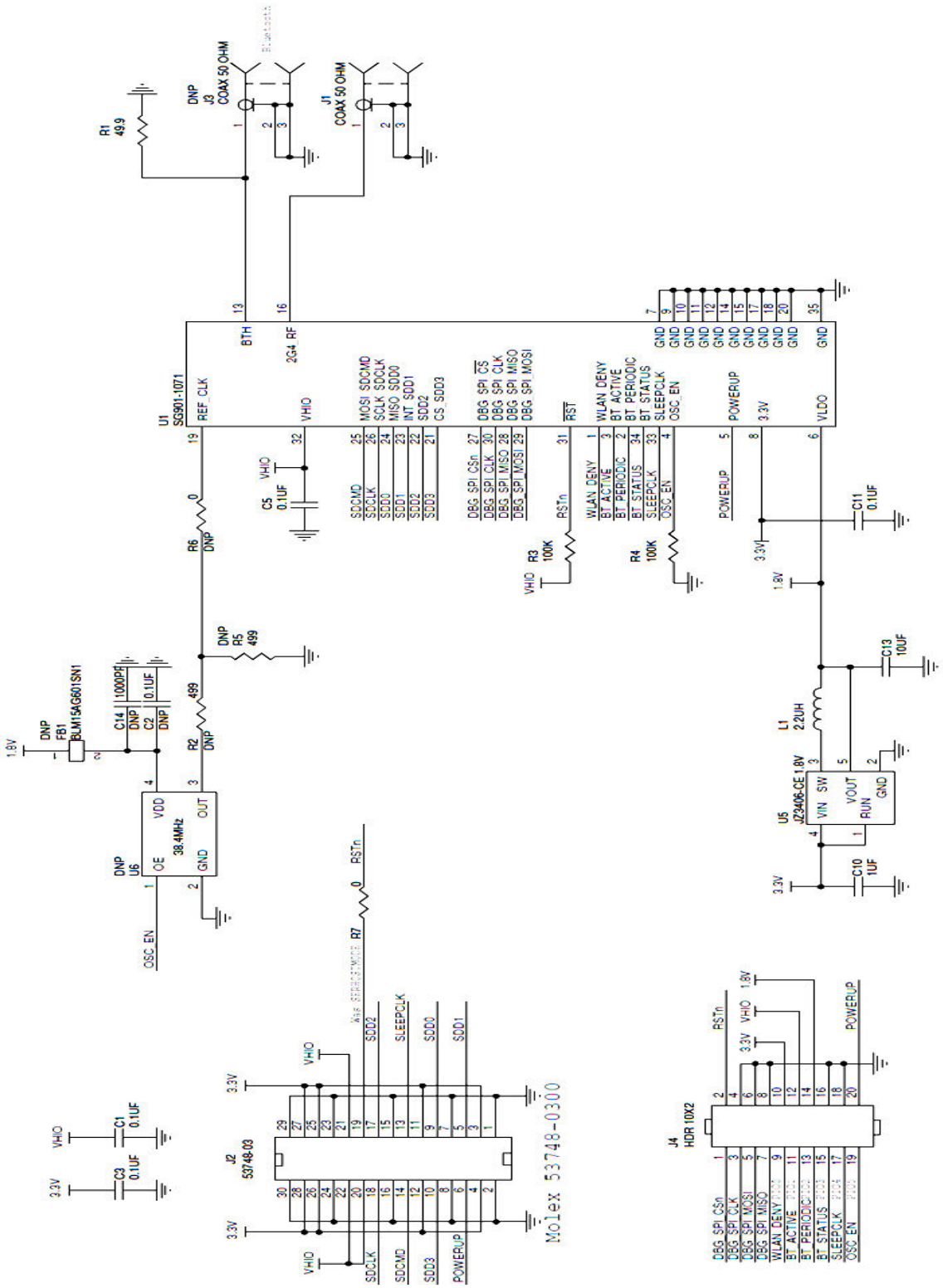
SDIO Host application

For SDIO applications simply insert the assembly into the SDIO socket available in most Host processor application/development boards. There are no external supplies or clocks required. The Kit is powered by the SDIO source in the Host development board.

SPI Host application

For SPI applications, the user is required to access the Bus using the connector JP1 in the adapter board. An external 3.3V power supply is required to power the evaluation kit assembly. Depending on the Host VHIO domain (Data Bus VOL, VOH, VIL, VIH), an external VHIO supply may be required if different than 3.3V. Please refer to the SPI pin descriptions. Use short wiring for the Bus connection.

Carrier Board Schematics



Adapter Board Schematics