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S1D13746 TV Out Mobile Graphics Engine

Hardware Functional Specification

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13746, TV-Out Embedded Memory Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Abbreviations and Acronyms

The following abbreviations and acronyms are used in this document:

All numbers are in decimal unless marked otherwise (b for binary, h for hexadecimal)
$k = 2^{10} = 1024$ when used with regards to memory
b = bit
B = Byte
bpp = bits-per-pixel
msb = Most Significant bit
lsb = Least Significant bit
IO = Input/Output
LUT = Look-Up Table
NC = No Connection
YYC = YUV to YUV Converter
YRC = YUV to RGB Converter
RYC = RGB to YUV Converter
VDP = Vertical Display Period
VNDP = Vertical Non-display Period
DDS = Digital Direct Synthesis
POUT = PLL Output

1.3 S1D13746 TV-Out Mobile Graphics Engine Family

The S1D13746 TV-Out Mobile Graphics Engine family currently includes the S1D13746B00 and the S1D13746B01/S1D13746F01. The following table describes the differences between these devices.

Table 1-1 S1D13746B0x Comparison

Device	Feature Differences
S1D13746B00	Base Design
S1D13746B01	All features of the S1D13746B00 plus: • GPIO interrupt and registers are asynchronous and fully functional in SLEEP mode. • Chrominance and Luminance filters for TV output improved from 11-TAP to 15-TAP to enhance Composite output. • Dot-Crawl elimination circuitry added for NTSC Composite mode. • Input and output scalers improved to provide sharper output image. • Input pre-scaler (decimation scaler) added to allow input image size of up to 3072x4092. • TV block changed to operate with flexible frequency range of 18MHz to 27MHz, and changed clock source for TV block to be selectable between CLKI/OSCI and PLL output divided by 2. This allows the possibility of running CLKI/OSCI from 1MHz to 54MHz range. • Square Pixel Correction Enable bit added to auto-scale the output window width to display square pixels. • Two more pin functions added to the TE (Tearing Effect) signal. • IO cells changed to Fail-Safe type. • Pull-Down resistor on the PWRSVE input removed.
S1D13746F01	All features of the S1D13746B01 in a QFP15 128-pin package.

2 Operational Overview

The S1D13746 is a Mobile Graphics Engine offering direct TV-output capability allowing for the display of multiple windows and orientations.

The S1D13746 contains a 312k byte display buffer. Input resolutions exceeding the memory space are automatically scaled down to fit. The final display output can be scaled-up and bordered to fit the standard TV resolutions as defined by PAL or NTSC.

TV output can be double-buffered to prevent image tearing during streaming video and also act as a frame-rate converter, allowing slow input video streaming while still maintaining PAL or NTSC output timing.

Input Data can come from a Host processor using an Intel 80 protocol or from a standard TFT display output (Parallel RGB Interface). The S1D13746 can be connected directly to a standard TFT display output. In this case, the registers are programmed using a Serial Interface and the S1D13746 converts the TFT output data appropriately for display on a TV.

All image data uses the Input/Output Window Size/Position registers and is accesses using the Display Memory Data Port. Subsequent windows are considered destructive overlays. Each window can have independent rotation and position characteristics.

The S1D13746 is designed to accept DMA burst accesses from an Intel 80 CPU interface. All accesses to the display buffer are handled through a Display Memory Data Port.

2.1 TV Support

The S1D13746 conforms to both the PAL and NTSC output standards with respect to resolution and output format. Both Composite and S-Video outputs formats are supported. The S1D13746 supports multiple RGB, YUV 4:2:2 and YUV 4:2:0 input formats. All data is converted and stored as YUV 4:2:0.

2.1.1 Writing Window Data

Window data can either be written by a Host processor via the Intel 80 Interface or input by the Parallel RGB Interface. For the Intel 80 processor, the windows can vary in size, For the Parallel RGB Interface, the window size is automatically determined by the horizontal and vertical input timings.

2.1.2 Scaling Features

- Host Input Data can be scaled-down to fit within the available memory.
  - The Input Scaler logic requires an input size, either programmed by the Host or calculated automatically if using the Parallel RGB Interface. The available memory is either the entire display buffer (312k bytes) or 156k bytes if the double buffer feature is enabled. The required scaling ratio from Input Size to memory is automatically calculated.
- Memory Output Data (intended for display on the TV) can be scaled-up for display on the TV (Display Output Scaler).
  - if the resulting scale-up does not equal full resolution as defined by the PAL or NTSC standards, then an automatic border is generated and the resulting image is centered within the border.
  - If displaying multiple images on the TV, the initial background image determines both the Scale-down ratio to memory and the Scale-up ratio to the display. These ratios are used by all other windows.
  - If displaying multiple images on the TV, all subsequent windows are referenced to the top-left of the (auto-centered) background image for position.

2.1.3 Window Rotation

SwivelView™ provides 90°, 180°, 270° counter-clockwise hardware rotation of the image window as written by the host. All windows can have independent rotation when writing to memory. No additional programming is necessary when enabling these modes.

2.1.4 Multiple TV Windows

Multiple “windows” can be destructively written to the TV display. If multiple windows are required, the first window written is considered the “background”. All subsequent windows are stored in memory “on-top” of the background image and are therefore considered destructive.

Multiple TV Windows with Transparency

Any destructive window can have a transparent color associated with it. Only those pixels that are not transparent are actually written to memory. The window is first scaled-down (if necessary) to fit in memory. After the scaler the pixels are compared to the 24-bit YUV value programmed for the transparent color.

There are three modes in which to use the transparent feature.

1. Normal Mode: if the resulting scaled pixels equal the transparent color, they are not written to memory. In this mode there will be color artifacts surrounding the non-transparent color.

2. Black/White Mode: in this mode, the transparent color is limited to black or white with the visible color being the opposite. In this mode any color artifacts are minimized by forcing all pixels to be either transparent or not.

3. Text Mode: in this mode, the transparent color intensity range calculated from the Transparency Color Registers determines if the pixel is transparent or not. This mode is similar to Black/White mode with the effect of removing more color artifacts.

2.1.5 Single TV Window

If only a single window is required, The S1D13746 can scale-down the input data to fit within the memory, scale-up for display on the TV, auto-center and Auto Border if the final output is not full screen.

2.1.6 TV Window Border Support

S1D13746 automatically generates a programmable border color around a window where the resulting image size (after scale-up) does not equal the TV output resolution (PAL or NTSC). The window is centered within the border.

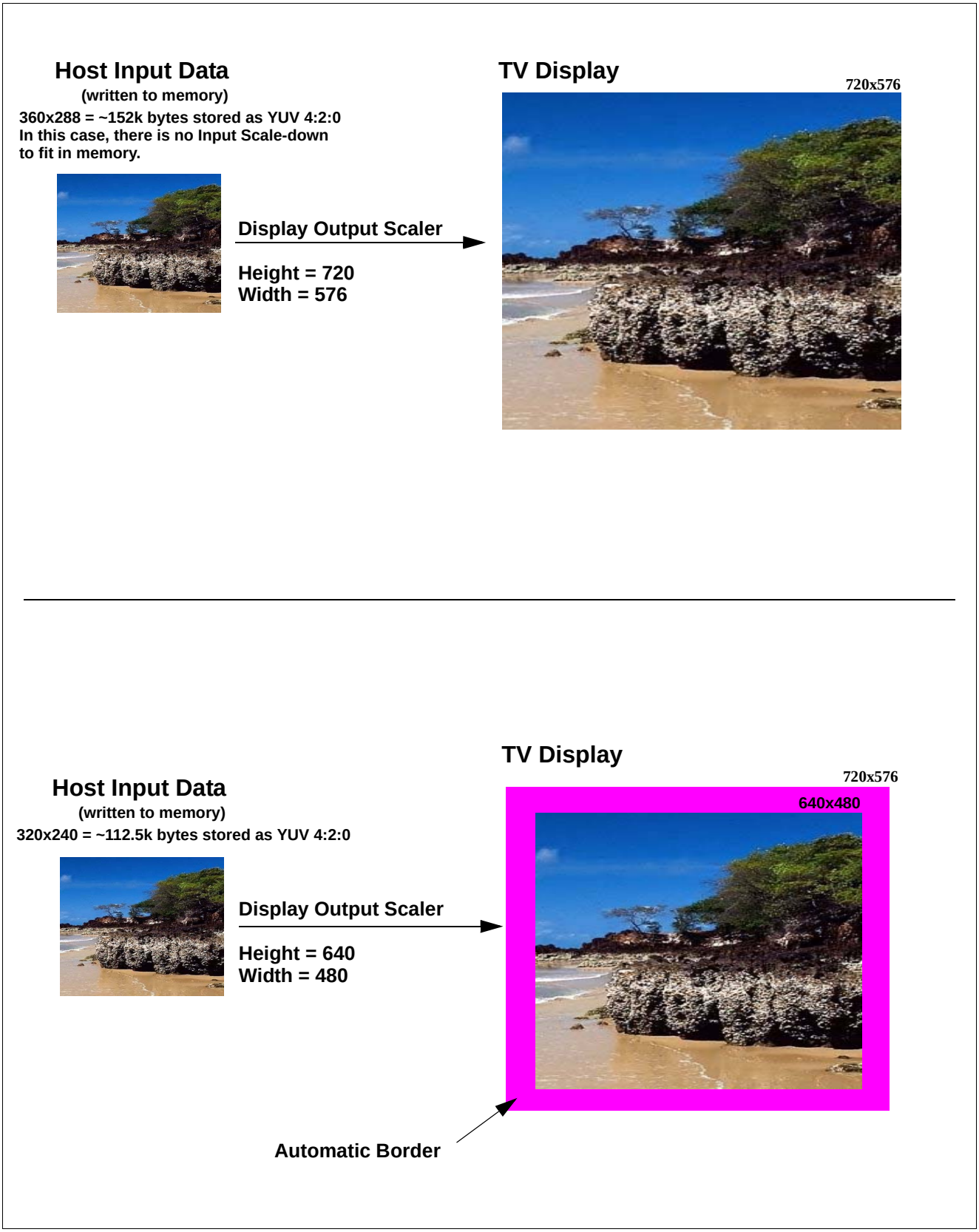
2.1.7 Double Buffered TV Window

A single TV window can be double buffered to prevent any visual tearing from a streaming input. This window can be the entire screen resolution or a just a portion.

When configuring a window for streaming video, the S1D13746 automatically double buffers the input data based on the window coordinates. If this window is only a portion of the screen, Buffer #1 is used for the “background” static portion and one of the buffered windows data. Buffer #2 is used only for the other double buffered window data and does not contain any static data from the background.

Interrupting a streaming window to update static information on the screen is permitted since the TV display pipe only uses data from a buffer that has been completely written. Therefore, a single buffer may be repeatedly displayed until the next buffer is ready. If the display pipe is currently using Buffer #2 when the Double Buffer is disabled, the display pipe reverts to using Buffer #1 since it is the only buffer containing the background information. Double-buffering supports the maximum resolutions as defined by the PAL and NTSC standard.

When Double Buffering is enabled, the memory is split into 2 banks of 156k bytes and the scale ratio from the input image to memory is increased to allow the image to fit inside 1/2 the previously available memory.


Host Input Data
(written to memory)
360x288 = ~152k bytes stored as YUV 4:2:0
In this case, there is no Input Scale-down
to fit in memory.
Display Output Scaler
Height = 720
Width = 576
TV Display
720x576
Host Input Data
(written to memory)
320x240 = ~112.5k bytes stored as YUV 4:2:0
Display Output Scaler
Height = 640
Width = 480
TV Display
720x576
640x480
Automatic Border

Host Input Data

(written to memory, Single Buffered)

720x576 = 607.5k bytes @ 4:2:0

Scaled-down to fit inside 312k bytes

514x412 = ~310k bytes @ 4:2:0

Host Input Data

(written to memory)

720x576

514x412 = ~312k bytes @ 4:2:0

Scaled-down to fit inside 312k bytes

Host Input Data (destructive window)

352x416

Scaled-down to fit inside background image

Memory Output Data

Scaled-up and Bordered

720x576

Host Input Data
(written to memory)

Scaled-down to fit inside 312k bytes

Host Input Data
(transparency enabled = black)

My Vacation

720x576

Memory Output Data

Scaled-up and Bordered

3 Features

3.1 Integrated Display Buffer

- Embedded 312k byte SRAM display buffer.

3.2 CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data).
- Parallel RGB Interface (display data only).
- Three Wire Serial Interface (register data only).
- Chip select is used to select the S1D13746. When inactive, input data/commands are ignored.

3.3 Input Data Formats

- RGB: 8:8:8, 6:6:6, 5:6:5, 3:3:2.
  - all RGB input data is converted and stored as YUV 4:2:0.
- YUV: 4:2:2, 4:2:0.
  - all YUV input data is converted and stored as YUV 4:2:0.

3.4 TV Display Support

- Composite Output for both PAL and NTSC TV standards.
- S-Video Output for both PAL and NTSC TV standards.
- Programmable 15-tap Chrominance / Luminance Filters.
- Wide-Screen Signalling support (ITU-R BT.1119-2, ETSI EN 300 294, IEC 61880, compliant).
- Closed Caption Support (CEA-608-B).

3.5 TV Display Features

- Input Data can:
  - be scaled-down to fit within available memory
  - be rotated.
  - have an associated transparent color
- Memory Output Data can be scaled-up for display on the TV
- TV image is automatically “bordered” to fit the output resolution, if not scaled to fit.
  - programmable YUV border color
  - auto-center
  - independent aspect ratio is available for Display Output Height/Width scaling factors
- Square pixel correction output width scaling

3.6 Image Enhancement Engine

- 3x3 Pixel Filter
- User defined coefficients
  - individual control for each YUV component
- Display effects include:
  - smooth, sharpen, blur, detail, edge enhance, emboss, contour, flicker filter, sepia

3.7 Clock Source

- Internal programmable PLL
- Single oscillator input: CLKI (determined by CNF2)

or

- Two-terminal Crystal support: OSCI, OSCO (determined by CNF2)

Note
An 18MHz to 27MHz clock is required by internal TV DDS logic in order to derive appropriate PAL and NTSC output timings. For any clock source other than 27MHz, the PLL should be programmed for 54MHz.

- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output)
  - output state = 0 when disabled

3.8 Miscellaneous

- Hardware / Software Power Save mode
  - Input pin to Enable/Disable Power Save Mode
- General Purpose Input/Output pins are available (GPIO[7:0])
  - INT pin associated with selectable GPIO inputs
- Package:

S1D13746B01B	PFBGA 100 pin (7mm x 7mm)
S1D13746F01A	QFP15 128 pin

4 Block Diagram

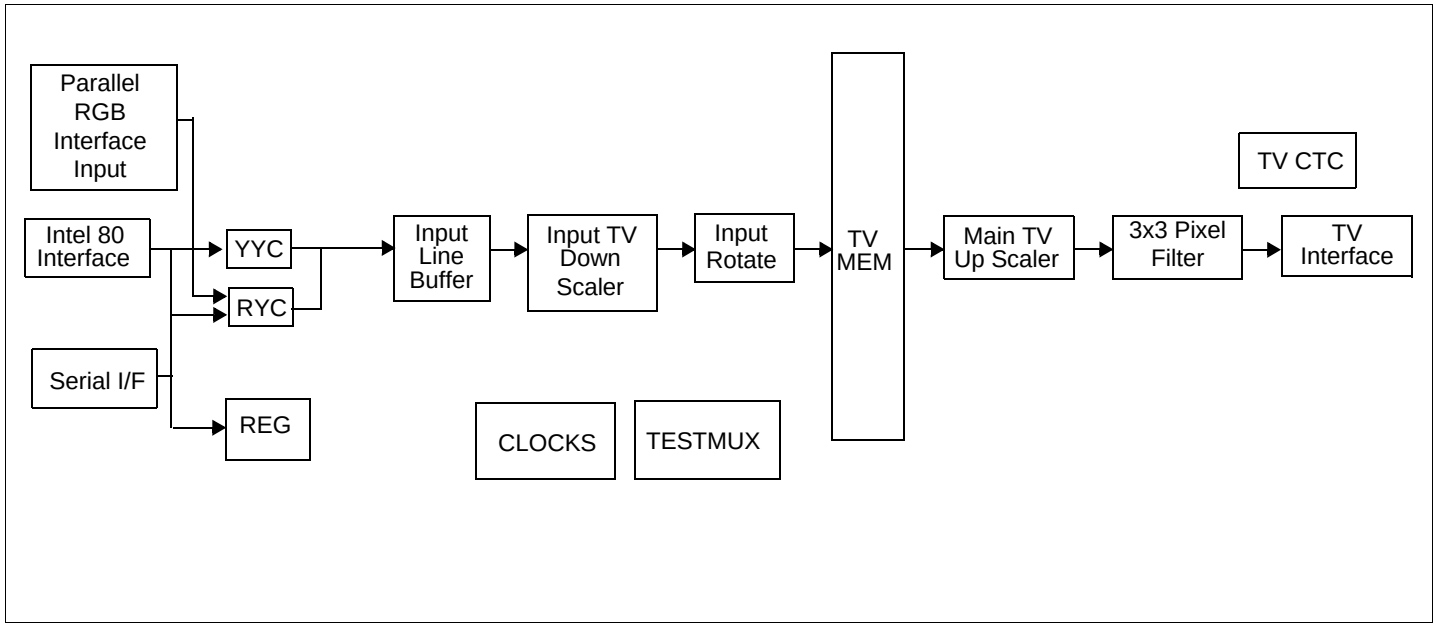


Figure 4-1: S1D13746 Block Diagram

5 Pinout

5.1 Package Pin Mapping

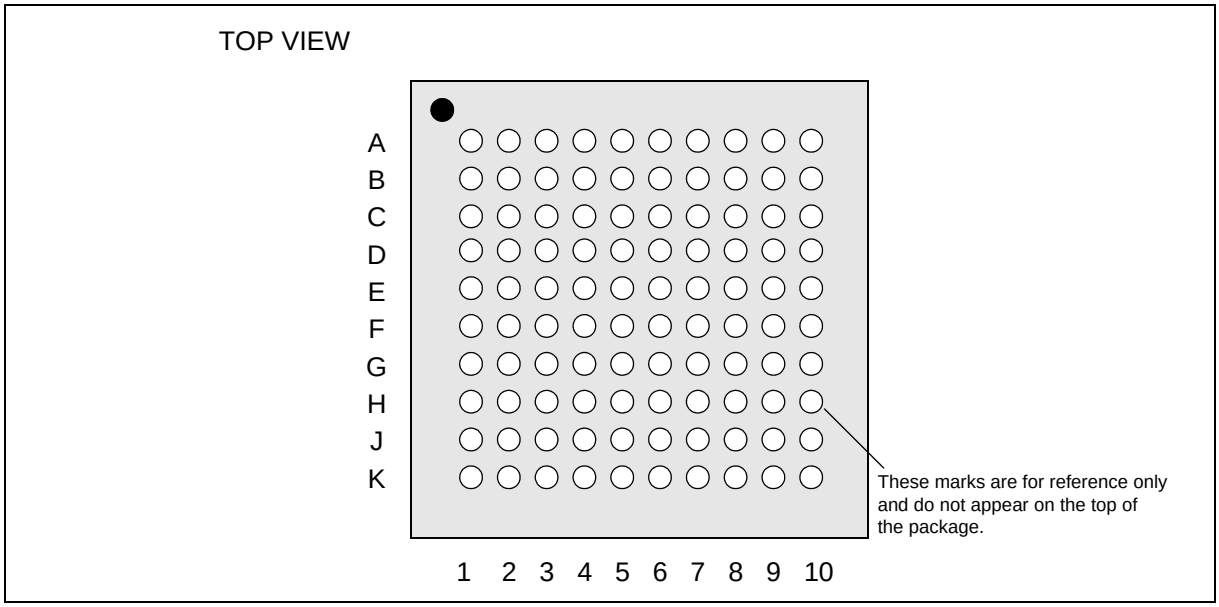


Figure 5-1: S1D13746 PFBGA 100-pin Pinout Diagram (Top View)

Table 5-1: S1D13746 PFBGA 100-pin Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10
A	NC	COREVDD	SCLK	SO	SI	VSS	PCLK	DE	VSS	NC
B	PWRSVE	TESTEN	GPIO7	CS#	GPIO1	GPIO0	TE	D/C#	COREVDD	MD15
C	SCANEN	TEST0	GPIO6	GPIO5	GPIO2	GPIO_INT	GPIO4	WE#	VSS	MD13
D	DACVEE	DACVCC	TEST2	SIOVDD	GPIO3	RESET#	IOVDD	MD11	MD12	MD9
E	BOUT	DACVCC	DACVEE	TEST1	CNF0	RD#	MD10	MD8	MD7	MD6
F	DACVEE	VADJ	DACVCC	VSS	CNF1	IOVDD	MD14	MD5	MD4	MD3
G	DACVEE	VREF	DACVEE	VSS	CNF3	CNF2	MD0	MD1	MD2	COREVDD
H	AOUT	DACVCC	DACVCC	VSS	VSS	IOVDD	VSS	IOVDD	CLKOUTEN	CLKOUT
J	DACVEE	DACVEE	DACVCC	IOVDD	COREVDD	OSCVSS	OSCVDD	VCP	VSS	CLKI
k	NC	NC	DACVEE	VSS	VSS	OSCI	OSCO	PLLVDD	PLLVSS	NC

Note

Pins marked as NC are not used and must be left unconnected.

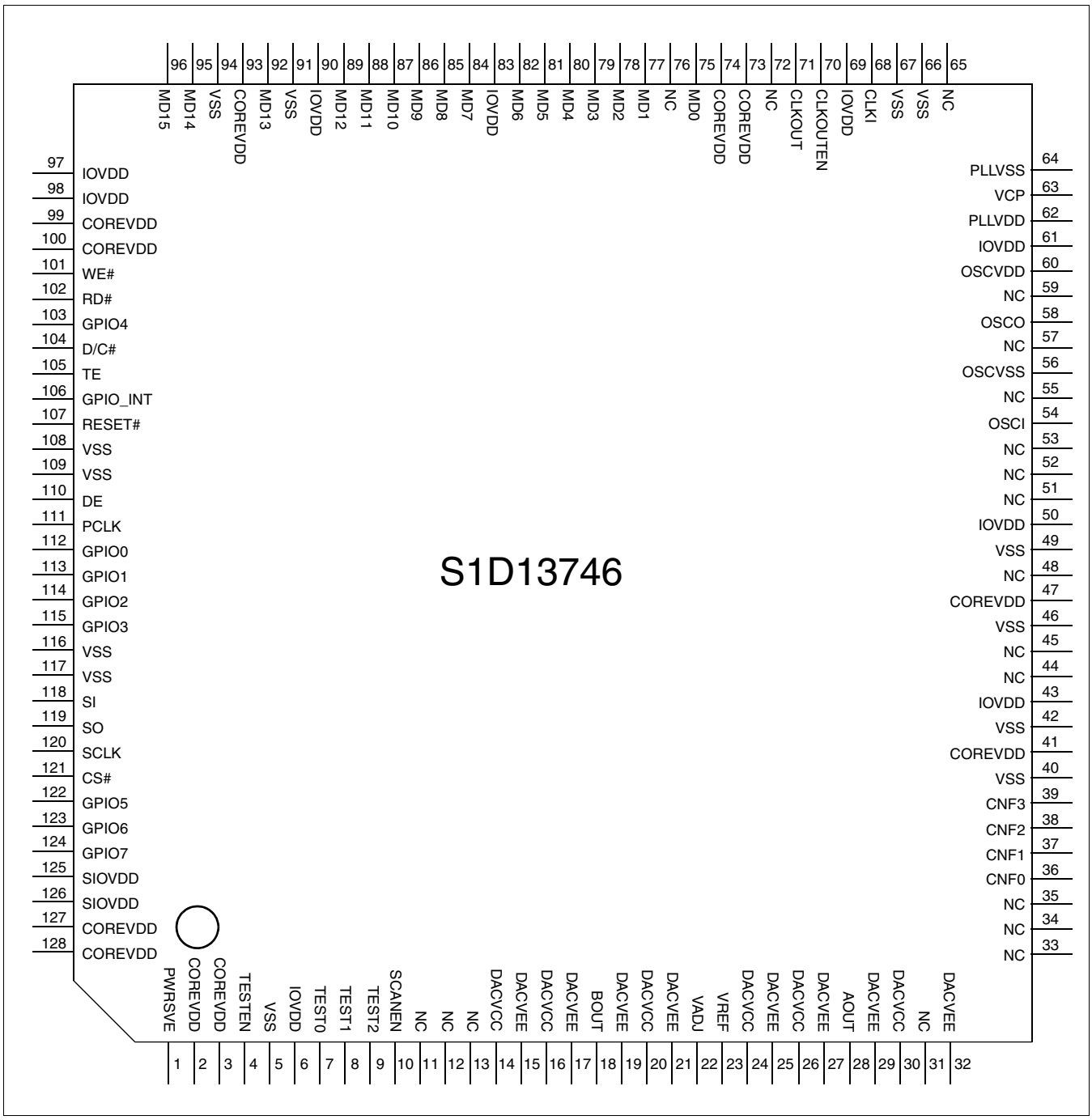


Figure 5-2: S1D13746 QFP15 128-pin (Top View)

Note

Pins marked as NC are not used and must be left unconnected.

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
AP	=	Analog power pin
G	=	Ground pin
AG	=	Analog ground pin

RESET# / Power Save Status

H	=	High level output
L	=	Low level output
Hi-Z	=	High Impedance

Table 5-3 Cell Description

Item	Description
HI	H System[1] LVCMOS[3] Input Buffer with Fail Safe
HIS	H System LVCMOS Schmitt Input Buffer with Fail Safe
HID	H System LVCMOS Input Buffer with pull-down resistor and Fail Safe
HO	H System LVCOMOS Output buffer with Fail Safe
HB	H System LVCMOS Bidirectional Buffer with Fail Safe
HBD	H System LVCMOS Bidirectional Buffer with pull-down resistor and Fail Safe
LIDS	L System[2] LVCMOS Schmitt Input Buffer with pull-down resistor
LITR	L System Transparent Input Buffer
LOTR	L System Transparent Output Buffer
AIO	Analog

[1] H System is IOVDD and PIOVDD (see Section 7, “D.C. Characteristics” on page 31).
[2] L System is COREVDD (see Section 7, “D.C. Characteristics” on page 31).
[3] LVCMOS is Low Voltage CMOS (see Section 7, “D.C. Characteristics” on page 31).

5.2.1 Intel 80 Host Interface

Table 5-2: Host Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
MD[15:0]	IO	B10, F7, C10, D9, D8, E7, D10, E8, E9, E10, F8, F9, F10, G9, G8, G7	96, 95, 92, 89, 88, 87, 86, 85, 84, 82, 81, 80, 79, 78, 77, 75	HB	IOVDD	Hi-Z	Hi-Z	This pin has multiple functions. • For the Intel 80 Interface these pins are the data lines MD[15:0], see Section 6.1, “Intel 80 Data Pins” on page 30. • For the Parallel RGB Interface these pins are the input data bits VD[17:2], see Section 6.2, “Parallel RGB Data Pins” on page 30
WE#	I	C8	101	HI	IOVDD	—	—	This pin has multiple functions. • For the Intel 80 Interface this input pin is the Write Enable signal (WE#) • For the Parallel RGB Interface this input pin is the data bit 1 (VD1)
RD#	I	E6	102	HI	IOVDD	—	—	This pin has multiple functions. • For the Intel 80 Interface this input pin is the Read Enable signal • For the Parallel RGB Interface this input pin is the data bit 0 (VD0)
CS#	I	B4	121	HI	SIOVDD	—	—	This input pin is the Chip Select signal for both the Intel 80 Host Interface as well as the Serial Interface.
D/C#	I	B8	104	HI	IOVDD	—	—	This pin has multiple functions. • For the Intel 80 Interface this input pin selects between address and data (D/C#) • For the Parallel RGB Interface this input pin is the Horizontal Sync (HS)
TE	IO	B7	105	HB	IOVDD	L	L	This pin has multiple functions. • For the Intel 80 Interface this pin is Tearing Effect. This pin reflects the VSYNC status of the display and can be used to indicate when it is safe to write new data from the Host in order to prevent visual tearing of an image. • For the Parallel RGB Interface this input pin is the Vertical Sync (VS)
PCLK	I	A7	111	HIS	IOVDD	—	—	This input pin is the Parallel RGB Interface PCLK input. If the Parallel RGB Interface is not used (CNF[1:0] = 01b or 11b) this pin should be connected to VSS.
DE	I	A8	110	HI	IOVDD	—	—	This input pin is the Parallel RGB Interface DE input. If the Parallel RGB Interface is not used (CNF[1:0] = 01b or 11b) this pin should be connected to VSS.

Table 5-2: Host Interface Pin Descriptions (Continued)

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
GPIO_INT	O	C6	106	HO	IOVDD	L	L	This pin is the interrupt output associated with GPIO pins when they are configured as inputs. When a GPIO interrupt occurs, this output pin is driven high. For details see the register descriptions for REG[F0h] ~ REG[FAh], in Section 11.3.9, “General Purpose IO Pins Registers” on page 117
RESET#	I	D6	107	HIS	IOVDD	—	—	This active low input sets all internal registers to the default state and forces all signals to their inactive states.

5.2.2 Serial Peripheral Interface (SPI)

Table 5-3: SPI Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
SO	IO	A4	119	HB	SIOVDD	Hi-Z	Hi-Z	This pin is the Serial Output. If the serial interface is not used (CNF[1:0] = 01b or 11b), this pin should be connected to either SIOVDD or VSS through a resistor .
SI	I	A5	118	HI	SIOVDD	—	—	This pin is the Serial Input. If the serial interface is not used (CNF[1:0] = 01b or 11b), this pin should be connected to VSS.
SCLK	I	A3	120	HIS	SIOVDD	—	—	This pin is the Serial Clock. If the serial interface is not used (CNF[1:0] = 01b or 11b), this pin should be connected to VSS.

5.2.3 TV Interface

Note
If unused, these pins should be left unconnected.

Table 5-4: TV Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
AOUT, BOUT	O	H1, E1	28, 18	AIO	DAC	—	—	These are the TV analog output pins. The TV outputs are designed to drive a double terminated 75Ω load (37.5 ohms). For further details, see Section 24.1, “DAC External Components” on page 184. When using Composite Video, AOUT is used and BOUT is left unconnected. When using S-Video, AOUT is the luminance signal and BOUT is the chrominance signal.
VREF	IO	G2	23	AIO	DAC	—	—	This input/output pin is the reference voltage for the DAC. The VREF Enable bit (REG[9Eh] bit 0) is used to determine whether external or internal VREF mode is selected. When REG[9Eh] bit 0 = 0b, external VREF mode is selected and 1.23 volts should be applied to this pin. When REG[9Eh] bit 0 = 1b, internal VREF mode is selected and this pin can be used during testing to confirm the output level is 1.23V. However, for normal operations, this pin should be left unconnected.
VADJ	IO	F2	22	AIO	DAC	—	—	This input/output is the reference current generation pin for the DAC. Connect a 2.06kΩ resistor (Rset) between VADJ and DACVEE. For further details, see Section 24.1, “DAC External Components” on page 184. When the IREF Enable bit = 0b (REG[9Eh] bit 1 = 0b), the internal generation of the reference current is disabled, and VADJ does not control reference current. There should be no problems with leaving the resistor connected.

5.2.4 Clocks

Note
For details on the clock structure, see Section 9, “Clocks” on page 59.

Table 5-5: Clock Input Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
CLKI	I	J10	68	HIS	IOVDD	—	—	This pin is the clock input when CNF2 = 0. When CNF2 = 1, this pin should be connected to VSS.
CLKOUT	O	H10	71	HO	IOVDD	Note 1	Note 1	This pin outputs the clock signal from either the CLKI pin or the OSCx pins, when enabled by the CLKOUTEN pin (see Section 9.1, “Clock Block Diagram” on page 59 for further information). When disabled, the output on this pin is low. **Note:** This output pin is not affected by the various power save modes.
CLKOUTEN	I	H9	70	HI	IOVDD	—	—	This input pin enables/disables the CLKOUT pin. When CLKOUTEN = 0, CLKOUT is disabled. When CLKOUTEN = 1, CLKOUT is enabled.
OSCO	O	K7	58	LOTR	OSCVDD	Note 2	Note 2	This output pin, along with OSCI, forms the 2-terminal crystal interface when CNF2 = 1. When the Internal Oscillator is not used or CNF2 = 0, This pin should be left unconnected.
OSCI	I	K6	54	LITR	OSCVDD	—	—	This input pin, along with OSCO, forms the 2-terminal crystal interface when CNF2 = 1. When the Internal Oscillator is not used or CNF2 = 0, This pin should be connected to OSCVDD or left unconnected.

Note
1. When CLKOUTEN = 1, this pin outputs CLKI (CNF2 = 1) or OSCI (CNF2 = 0). When CLKOUTEN = 0, this pin is L.
2. When CNF2=1, this pin is active. When CNF2=0, this pin is H.

5.2.5 Miscellaneous

Table 5-6: Miscellaneous Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
CNF[3:0]	I	G5, G6, F5, E5	39, 38, 37, 36	HI	IOVDD	—	—	These inputs are used for power-on configuration. For details, see Section 5.3, “Summary of Configuration Options” on page 29. **Note: These pins must be connected directly to IO V_{DD} or V_{SS}.**
TESTEN	I	B2	4	LIDS	IOVDD	0	—	This pin is the Test Enable input and is used for production test only. This pin should be left unconnected for normal operations.
GPIO[7:5]	IO	B3, C3, C4	124, 123, 122	HBD	SIOVDD	0	active	These pins are General Purpose IO pins. These pins have internal pull-down resistors which can be controlled using REG[FAh].
GPIO[4:0]	IO	C7, D5, C5, B5, B6	103, 115, 114, 113, 112	HBD	IOVDD	0	active	These pins are General Purpose IO pins. These pins have internal pull-down resistors which can be controlled using REG[FAh].
PWRSVE	I	B1	1	HI	IOVDD	—	—	This input pin enables/disables the selected Power Save Mode (Sleep or Standby). REG[2Eh] bit 7 allows the state of this pin to be ORed with either the Sleep Mode Enable bit (REG[2Eh] bit 1) or the Standby Mode Enable bit (REG[2Eh] bit 0). Note: This pin must be driven by an external source or terminated to VSS so that it is not floating.
TEST[2:0]	I	D3, E4, C2	9, 8, 7	HID	IOVDD	—	—	These input pins are for production test only and should be left unconnected for normal operations.
SCANEN	I	C1	10	HID	IOVDD	—	—	This pin is the Scan Enable input and is used for production test only. This pin should be left unconnected for normal operations.
VCP	I	J8	63	LITR	PLLVDD	—	—	This input pin is for production test only and should be left unconnected for normal operations.

5.2.6 Power And Ground

Table 5-7: Power And Ground Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	Description
COREVDD	P	A2, B9, G10, J5	2, 3, 41, 47, 73, 74, 93, 99, 100, 127, 128	P	Core power supply
IOVDD	P	D7, F6, H6, H8, J4	6, 43, 50, 61, 69, 83, 90, 97, 98	P	IO power supply for the host interface
SIOVDD	P	D4	125, 126	P	IO power supply for the serial interface
VSS	G	A6, A9, C9, F4, G4, H4, H5, H7, J9, K4, K5	5, 40, 42, 46, 49, 66, 67, 91, 94, 108, 109, 116, 117	P	GND
OSCVDD	P	J7	60	P	IO power supply for the Oscillator (2.5v)
OSCVSS	P	J6	56	P	GND for the Oscillator
PLLVDD	AP	K8	62	P	PLL Power Supply
PLLVSS	AG	K9	64	P	GND for PLL
DACVCC	AP	D2, E2, F3, H2, H3, J3	14, 16, 20, 24, 26, 30	P	DAC Analog Power Supply
DACVEE	AG	D1, E3, F1, G1, G3, J1, J2, K3	15, 17, 19, 21, 25, 27, 29, 32	P	GND for DAC Analog

5.3 Summary of Configuration Options

These pins are used for power-up configuration and must be connected directly to IOV_{DD} or V_{SS}. The status of these pins can be read in REG[02h] using the CNF[3:0] Status bits.

Table 5-8: Summary of Power-On/Reset Options

Configuration Input	Power-On/Reset State	
	1 (connected to IOV_{DD})	**0 (Connected to V_{SS})**
CNF[1:0]	Select Host Interface as follows: **CNF1** **CNF0** **Host Bus** 0 0 3-Wire Serial Host Interface with Parallel RGB Interface 0 1 8-Bit Intel 80 1 0 SPI Host Interface with Parallel RGB Interface 1 1 16-Bit Intel 80	
CNF2	2-Terminal Crystal used as input clock (OSCI, OSCO pins)	Oscillator used as input clock (CLKI pin)
CNF3	Reset Filter = 5 ps (clock must be present)	Reset Filter = 43 ns (no clock needed)

Note

When CNF1 = 0, all register accesses are 8-bit only.
When CNF1 = 1 (16-bit), all register accesses are 8-bit ONLY (most significant byte on the data bus is ignored) except to the Display Memory Data Port (REG[A0h]. Access to the Display Memory Data Port is 16-bit.

6 Pin Mapping

6.1 Intel 80 Data Pins

Intel 80 data pin mapping is controlled by CNF[1:0]. For details on CNF[1:0], see Section 5.3, “Summary of Configuration Options” on page 29.

Table 6-1: Intel 80 Data Pin Mapping

Pin Name	16-Bit Data CNF[1:0] = 11b	8-Bit Data CNF[1:0] = 01b
MD15	MD15	Connect to ground through pull-down resistors (eight used)
MD14	MD14	
MD13	MD13	
MD12	MD12	
MD11	MD11	
MD10	MD10	
MD9	MD9	
MD8	MD8	

Pin Name	16-Bit Data CNF[1:0] = 11b	8-Bit Data CNF[1:0] = 01b
MD7	MD7	MD7
MD6	MD6	MD6
MD5	MD5	MD5
MD4	MD4	MD4
MD3	MD3	MD3
MD2	MD2	MD2
MD1	MD1	MD1
MD0	MD0	MD0

6.2 Parallel RGB Data Pins

Table 6-2: Parallel RGB Data Pin Mapping

S1D13746 Pin Name	RGB Pin Name	RGB Function
MD15	VD17	R5
MD14	VD16	R4
MD13	VD15	R3
MD12	VD14	R2
MD11	VD13	R1
MD10	VD12	R0
MD9	VD11	G5
MD8	VD10	G4
MD7	VD9	G3
MD6	VD8	G2
MD5	VD7	G1

S1D13746 Pin Name	RGB Pin Name	RGB Function
MD4	VD6	G0
MD3	VD5	B5
MD2	VD4	B4
MD1	VD3	B3
MD0	VD2	B2
WE#	VD1	B1
RD#	VD0	B0
D/C#	HS	HS
TE	VS	VS
DE	DE	DE
PCLK	PCLK	PCLK

7 D.C. Characteristics

7.1 Absolute Maximum Ratings

Table 7-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
COREVDD	Core Supply Voltage	- 0.3 ~ 2.0	V
PLLVDD	PLL Supply Voltage	- 0.3 ~ 2.0	V
IOVDD	Host IO Supply Voltage	COREVDD ~ 4.0	V
SIOVDD	Serial IO Supply Voltage	COREVDD ~ 4.0	V
OSCVDD	Crystal Oscillator Supply Voltage	COREVDD ~ 4.0	V
DACVCC	DAC Analog Supply Voltage	COREVDD ~ 4.0	V
V_{IN}	Input Voltage	- 0.3 ~ IOVDD + 0.5	V
V_{IN_F}	Input Voltage (Fail Safe I/O)	- 0.3 ~ 4.0	V
V_{OUT}	Output Voltage	- 0.3 ~ IOVDD + 0.5	V
I_{OUT_IO}	Digital Output Current	±10	mA
I_{OUT_DAC}	DAC Output Current	±50	mA
T_{STG}	Storage Temperature	-65 ~ 150	°C

7.2 Recommended Operating Conditions

The following characteristics are for: VSS = PLLVSS = OSCVSS = DACVEE = 0V

Table 7-2: Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
COREVDD	Core Supply Voltage	1.35	1.50	1.65	V
PLLVDD	PLL Supply Voltage				
IOVDD	Host IO Supply Voltage	1.62	—	3.60	V
SIOVDD	Serial IO Supply Voltage	1.62	—	3.60	V
OSCVDD	Crystal Oscillator Supply Voltage	1.62	—	3.60	V
DACVCC	DAC Analog Supply Voltage	2.70	3.00	3.30	V
V_{IN}	Input Voltage	0	—	IOVDD	V
V_{IN_F}	Input Voltage (Fail Safe I/O)	0	—	3.90	V
T_{OPR}	Operating Temperature	-40	25	85	°C

7.3 Electrical Characteristics

The following characteristics are for the Recommended Operation Conditions.

Table 7-3: Electrical Characteristics IOVDD or SIOVDD or OSCVDD = 1.62V to 3.60V, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IZ}	Input Leakage Current	—	-1	—	1	pA
I_{OZ}	Off State Leakage Current	—	-1	—	1	pA
IOV_{OH}	High Level Output Voltage	IOVDD = Min. IOH = -1.8mA	IOVDD - 0.4	—	—	V
IOV_{OL}	Low Level Output Voltage	IOVDD = Min. IOL = 1.8mA	—	—	0.4	V
V_{IH}	High Level Input Voltage	LVCMOS Level	IOVDD x 0.7	—	IOVDD + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level	-0.3	—	IOVDD x 0.3	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	IOVDD x 0.4	—	IOVDD x 0.7	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	IOVDD x 0.25	—	IOVDD x 0.55	V
GV	Hysteresis Voltage	LVCMOS Schmitt	IOVDD x 0.1	—	—	V
R_{PD}	Pull-down Resistance	VI = IOVDD	20	—	244	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, IOVDD = 0V	—	—	8	pF

Table 7-4: Power Consumption

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{QHVDD}	IO, OSC Quiescent Current	—	—	1	—	pA
I_{QLVDD}	Core, PLL Quiescent Current	—	—	20	—	pA
I_{QDAC}	DAC Quiescent Current	—	—	1	—	pA
I_{IO}	IOVDD Operation Current	—	—	—	5	mA
I_{OSC}	OSCVDD Operation Current	27MHz Crystal	—	600	—	pA
I_{CORE}	COREVDD Operation Current	—	—	—	33	mA
I_{PLL}	PLLVDD Operation Current	f = 54MHz	—	0.8	2.0	mA
I_{DAC}	DACVCC Operation Current	S-Video	—	90	100	mA
		Composite	—	45	50	mA

7.4 DAC Characteristics

The following characteristics are for: DACVCC = 2.7V to 3.3V, VSS = PLLVSS = OSCVSS = DACVEE = 0V, T_{OPR} = -40 to 85 °C, R_L = 37.5z , C_L = 30pF, R_{ADJ} = 2060z , VREF = Open.

Table 7-5: DAC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	Resolution	—	—	10	—	bits
	Sample Rate	—	—	27	—	MHz
	Clock Duty Cycle	—	40	50	60	%
	Minimum Output Voltage	Zero Scale	-0.05	0	0.05	V
	Maximum Output Voltage	Full Scale	1.17	1.30	1.43	V
	Differential Nonlinearity	—	-1	—	1	LSB
	Integral Nonlinearity	—	-3	—	3	LSB

Note

If the TV outputs from AOUT or BOUT are not connected to a double termination of 75 ohms (i.e. the 75 ohm load resistor and an external 75 ohm load) but only single terminated with a single 75 ohm load, the output voltage level is double.

7.5 Power Estimation Guidelines

The following information summarizes the power estimation guidelines for each of the three possible modes: Active, Standby Mode, and Sleep Mode.

These guidelines are based on CLKI/OSC = 27 MHz, SYSCLK = 54 MHz, and results will vary based on user environment.

Table 7-6: Typical Power Consumption

Active Display (Note 1)	Current Consumption	Comments
Core (1.5V)	15mA / 20mA	Intel 80 Host / Parallel RGB Host
PLL (1.5V)	528uA	—
DAC(3.0V)	48mA	Composite video output (REG[40h] bit 4 = 0b)
	92mA	S-Video output (REG[40h] bit 4 = 1b)
OSCVDD(1.8V)	565uA	if used, otherwise zero
IOVDD(1.8V)[4]	80uA / 900uA	Host Activity / CLKOUT enabled
SIOVDD(1.8V)[4]	15uA	Serial host register accesses

Standby Mode Enabled (Note 2)	Current Consumption	Comments
Core (1.5V)	820uA	—
PLL (1.5V)	528uA	—
DAC(3.0V)	0	—
OSCVDD(1.8V)	565uA	if used, otherwise zero

Sleep Mode Enabled (Note 3)	Current Consumption	Comments
Core (1.5V)	330uA / 15 uA	CLKI Active / CLKI Grounded
PLL (1.5V)	0	—
DAC(3.0V)	0	—
OSCVDD(1.8V)	565uA	if used, otherwise zero

Note

1. Active Display Mode is when the PWRSVE pin is low **and** both the Sleep Mode Enable bit (REG[2Eh] bit 1) and Standby Mode Enable bit (REG[2Eh] bit 0) = 0b.
2. Standby Mode is when the Standby Mode Enable bit = 1b (REG[2Eh] bit 0 = 1b) **or** the PWRSVE pin is high when the PWRSVE Input Pin Function is configured for Standby Mode (REG[2Eh] bit 7 = 1b).
3. Sleep Mode is when the Sleep Mode Enable bit = 1b (REG[2Eh] bit 1 = 1b) **or** the PWRSVE pin is high when the PWRSVE Input Pin Function is configured for Sleep Mode (REG[2Eh] bit 7 = 0b).
4. IOVDD/SIOVDD depends on activity on the Intel 80 host interface, Serial Host Interface, or GPIOs and are not affected by Standby or Sleep Mode.

8 A.C. Characteristics

Conditions:

IOVDD = 1.62V to 3.60V
T_{OPR} = -40 · C to 85 · C
T_{rise} and T_{fall} for all inputs except Schmitt and CLKI must be ≤ 50 ns (10% ~ 90%)
T_{rise} and T_{fall} for all Schmitt must be ≤ 5 ms (10% ~ 90%)
C_L = 8pF ~ 30pF (MD[15:0])
C_L = 15pF (TE, GPIO_INT, CLKOUT)
C_L = 30pF (GPIO Interface)

8.1 Clock Timing

8.1.1 Input Clocks

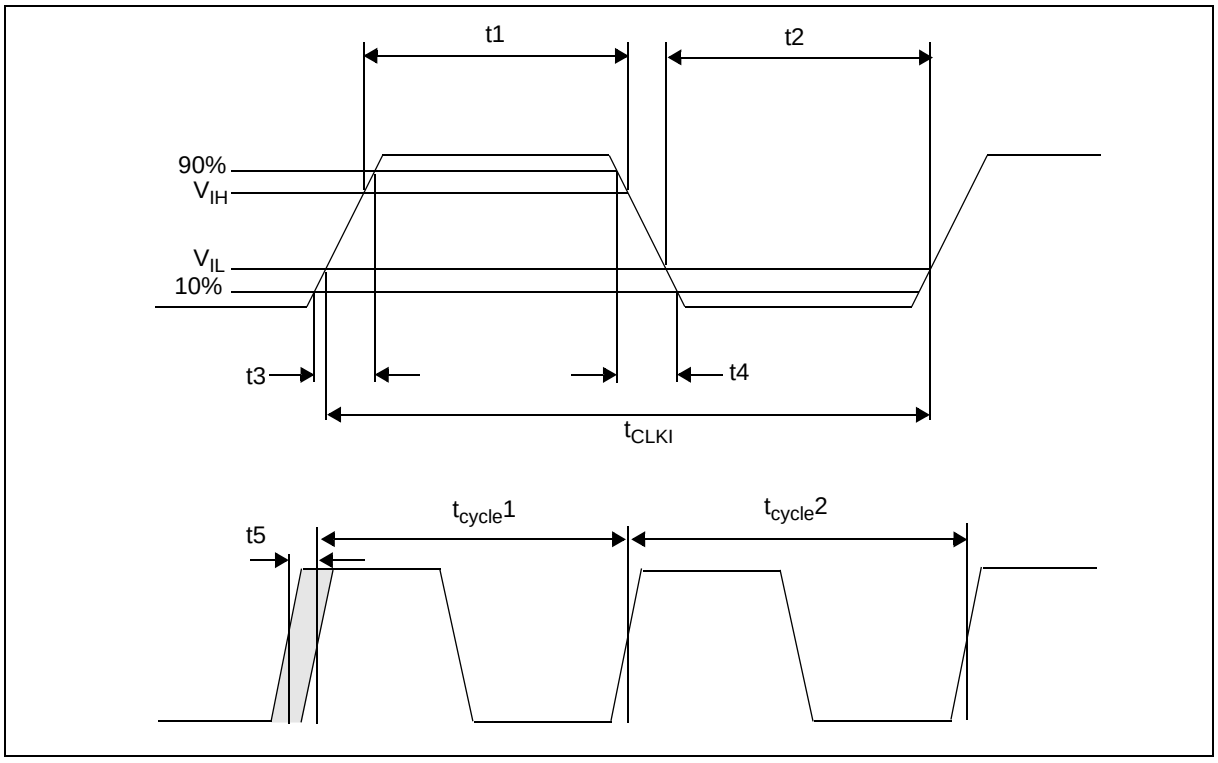


Figure 8-1 Clock Input Required (PLL)

Table 8-1: Clock Input Requirements (CLKI)

Symbol	Parameter	Min	Typ	Max	Units
f_{CLKI}	Input clock frequency	18	27	27	MHz
t_{CLKI}	Input clock period	—	$1/f_{CLKI}$	—	ps
t1	Input clock pulse width high	0.45	—	0.55	t_{CLKI}
t2	Input clock pulse width low	0.45	—	0.55	t_{CLKI}
t3	Input clock rise time (10% - 90%)	—	—	5	ns
t4	Input clock fall time (90% - 10%)	—	—	5	ns
t5	Input clock period jitter (see notes 2 and 4)	-300	—	300	ps
t6 (see note 1)	Input clock cycle jitter, NTSC TV output (see notes 3 and 4)	-50	—	50	ppm
	Input clock cycle jitter, PAL TV output (see notes 3 and 4)	-25	—	25	ppm

1. $t6 = t_{cycle1} - t_{cycle2}$
2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
3. The input clock cycle jitter is the difference in period between adjacent cycles.
4. The jitter characteristics must satisfy both the t5 and t6 characteristics

8.1.2 OSC Clock

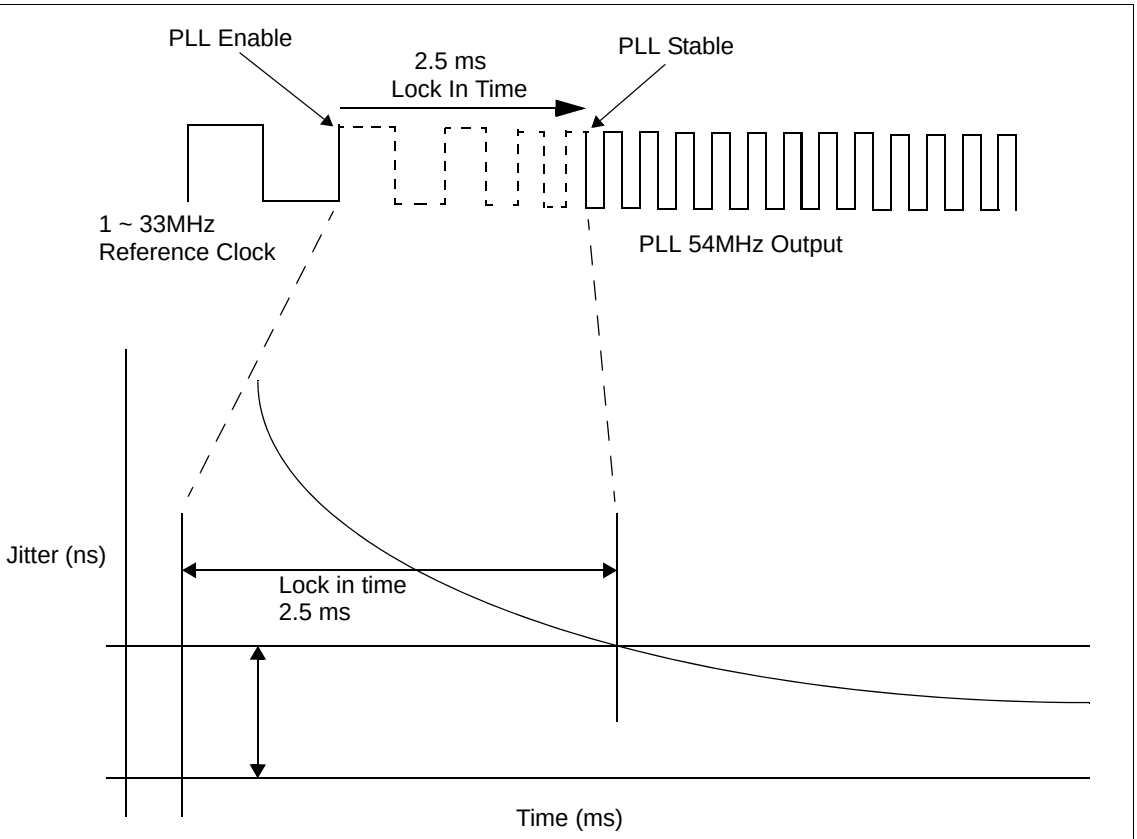
Table 8-2: OSC Crystal Clock Requirements (OSC)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC}	OSC Crystal clock frequency	18	27	27	MHz
t_{OSC}	OSC Crystal clock period	—	$1/f_{OSCI}$	—	ps

8.1.3 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.



The PLL frequency will ramp between the OFF state and the programmed frequency.
To guarantee the lowest possible clock jitter, 2.5 ms is required for stabilization.

Note: PLL frequency = 54MHz

Figure 8-2: PLL Start-Up Time

Table 8-3: PLL Characteristics

Symbol	Parameter	Min	Typ	Max	Units
f_{PLLI}	PLL input clock frequency after M-Divider	1	—	2	MHz
f_{PLLI2}	PLL input clock frequency before M-Divider	1	—	33	MHz
f_{PLLO}	PLL output clock frequency	—	54	—	MHz
t_{PJref}	PLL output clock period jitter	-3	—	3	%
t_{PDuty}	PLL output clock duty cycle	30	—	70	%
t_{PStal}	PLL output stable time	—	—	2.5	ms

8.2 RESET# Timing

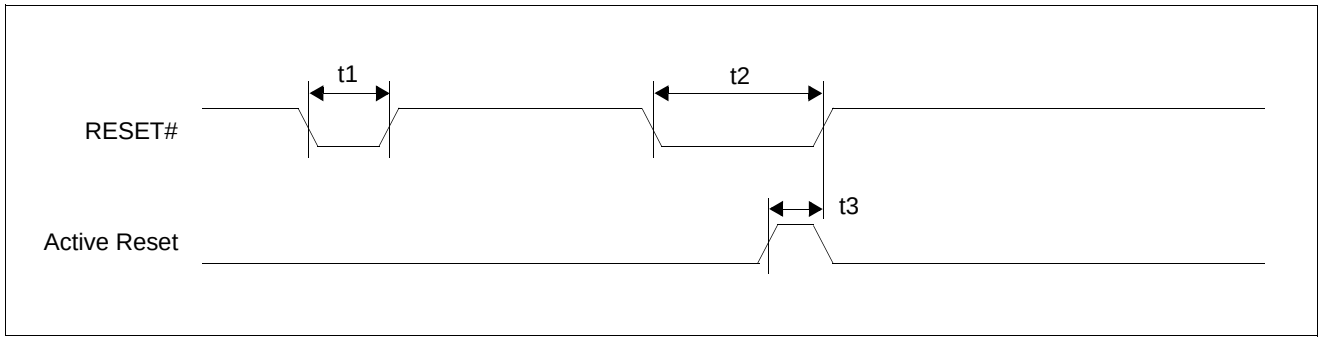


Figure 8-3 S1D13746 RESET# Timing

Table 8-4 S1D13746 RESET# Timing

CNF3	Symbol	Parameter	Min (note 1)	Max (note 2)	Units
0	t1	Reset Pulse Width to be ignored when 5ps Reset Filter is disabled	–	43	ns
	t2	Active Reset Pulse Width when 5ps Reset Filter is disabled	150	–	ns
1	t1	Reset Pulse Width to be ignored when 5ps Reset Filter is enabled	–	5.01	ps
	t2	Active Reset Pulse Width when 5ps Reset Filter is enabled	5.20	–	ps
	t3	t2 - t1	–	–	–

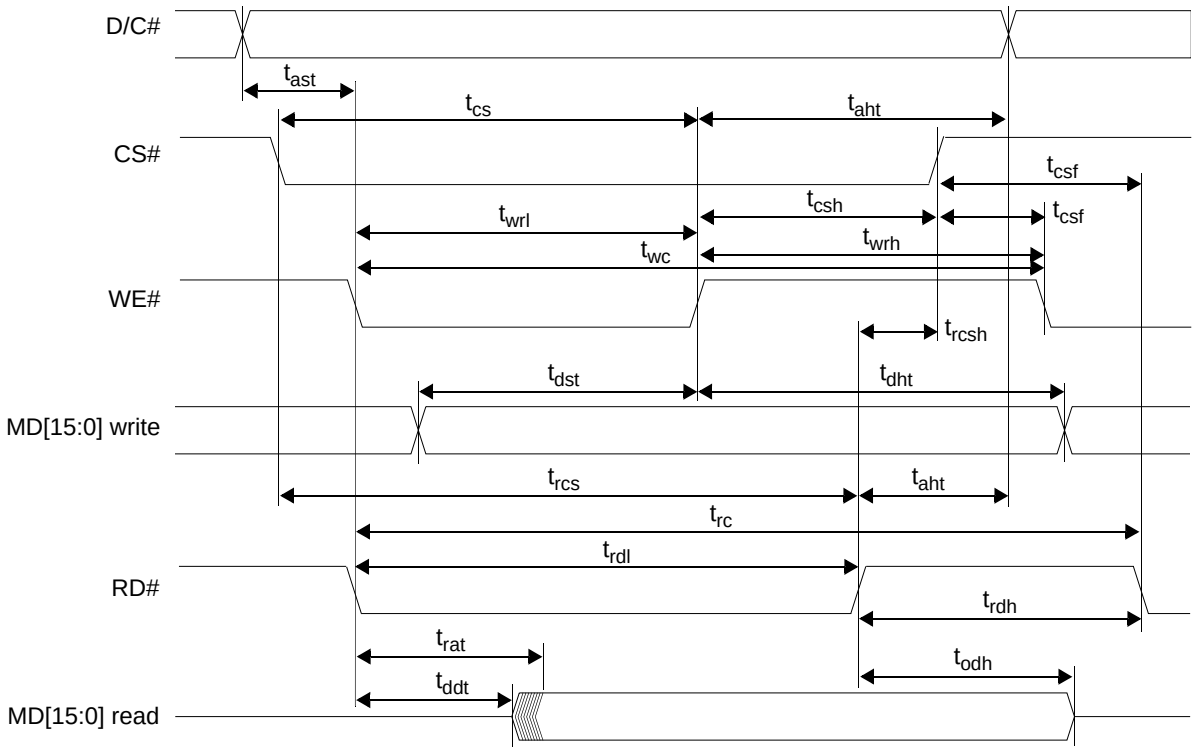
1. Min numbers are based on the minimum recommended operating conditions (see Section 7.2, “Recommended Operating Conditions” on page 31)
2. Max numbers are based on the maximum recommended operating conditions (see Section 7.2, “Recommended Operating Conditions” on page 31)

Note

The 5ps Reset Filter requires CLKI and timing is based on a CLKI frequency of 27MHz.

8.3 Host interface Timing

8.3.1 Intel 80 Interface Timing



Note: The D/C# input pin is used to distinguish between Address and Data.

Note: The CS# pin can be kept low between write pulses as the register addresses will auto increment. The register address will auto increment in word increments for all register access except the Display Memory Data Port. Writes to the Display Memory Data Port will not increment the register address to support burst data writes to memory.

Figure 8-4: Intel 80 Input A.C. Characteristics

Table 8-5: Intel 80 Input A.C. Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/C#	t_{ast}	Address setup time	3.0	—	ns	
	t_{aht}	Address hold time	1.0	—	ns	
CS#	t_{cs}	Chip Select setup time (write)	2.0 + t_{wrl}	—	ns	
	t_{rcs}	Chip Select setup time (read)	1.0 + t_{rdl}	—	ns	
	t_{csf}	Chip Select Wait time	10.0	—	ns	
	t_{csh}	Chip select hold time (write)	0	—	ns	
	t_{rcsh}	Chip select hold time (read)	0	—	ns	
WE#	t_{wc}	Write cycle (falling edge to next falling edge)	2SYSCLK	—	ns	
	t_{wrh}	Pulse high duration	Note 1	—	ns	
	t_{wrl}	Pulse low duration	1.0	—	ns	
RD#	t_{rc}	Read cycle for Registers	28.0	—	ns	
	t_{rdh}	Pulse high duration	4.0	—	ns	
	t_{rdl}	Pulse low duration for Registers	24.0	—	ns	
MD[15:0]	t_{dst}	Data setup time	4.0	—	ns	For maximum CL=30pF For minimum CL=8pF
	t_{dht}	Data hold time	3.0	—	ns	
	t_{rat} (See note)	Read falling edge to Data valid for Registers	5.5	22.5	ns	
	t_{odh} (See note)	Read hold time	11.0	36.5	ns	
	t_{ddt} (See note)	Read falling edge to Data driven	4.0	19.0	ns	

1. t_{wrh} min = long enough to satisfy t_{wc}

Note

Definition of transition time to Hi-Z state.

Due to the difficulty of Hi-Z impedance measurement for high speed signals, transition time from H/L to Hi-Z specified as follows.

H to Hi-Z delay time: t_{pHZ}, delay time when a gate voltage of final stage of the Pch-MOSFET turns to 0.8 x IOVDD (Pch-MOSFET is off). Total delay time to Hi-Z is calculated as following equation;

Internal logic delay + t_{pHZ} (from H to Hi-Z)

L to Hi-Z delay time: t_{pLZ}, delay time when a gate voltage of final stage of the Nch-MOSFET turns to 0.2 x IOVDD (Nch-MOSFET is off). Total delay time to Hi-Z is calculated as following equation;

Internal logic delay + t_{pHZ} (from H to Hi-Z)

The functional model of a final stage of the Tri state Output Cell is shown in Figure 8-5: “Definition of Transition Time to Hi-Z State”.

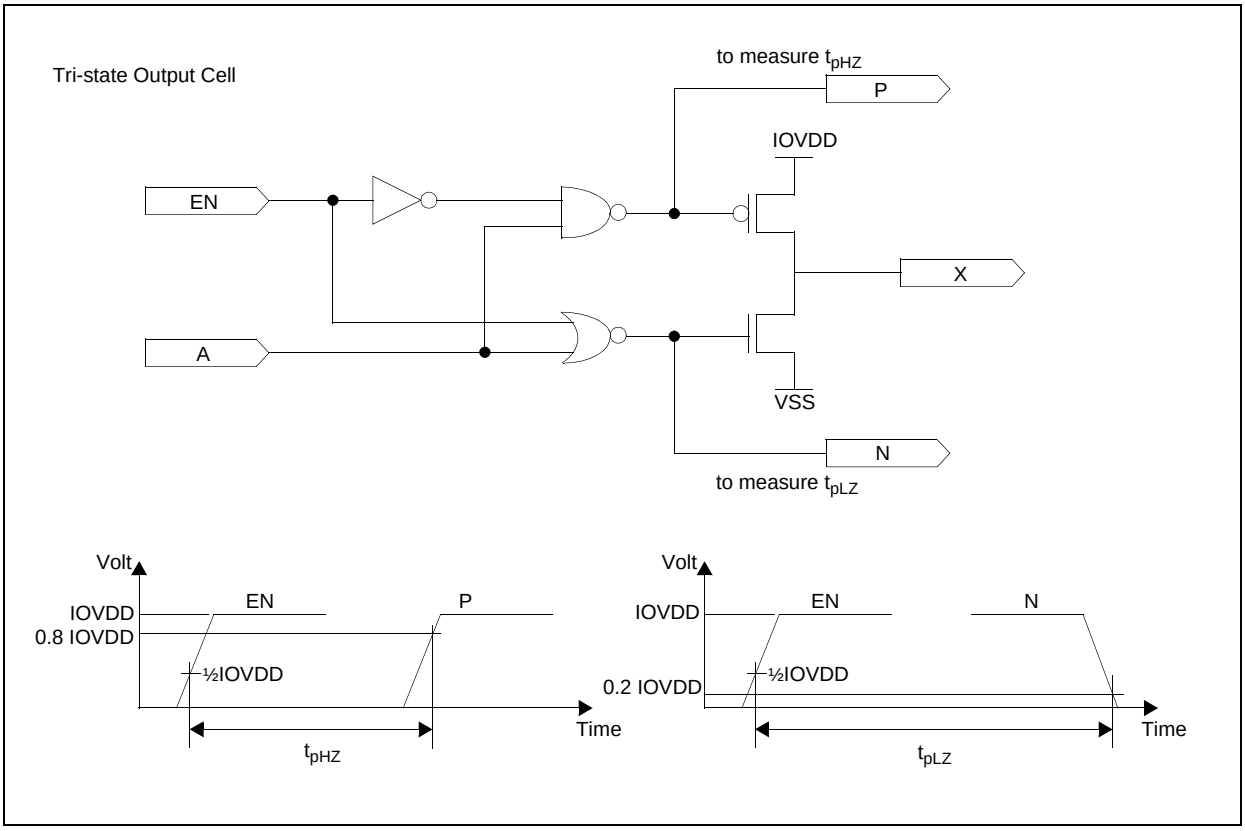


Figure 8-5: Definition of Transition Time to Hi-Z State

8.4 Serial Interface Timing

8.4.1 3-Wire Serial Interface Timing

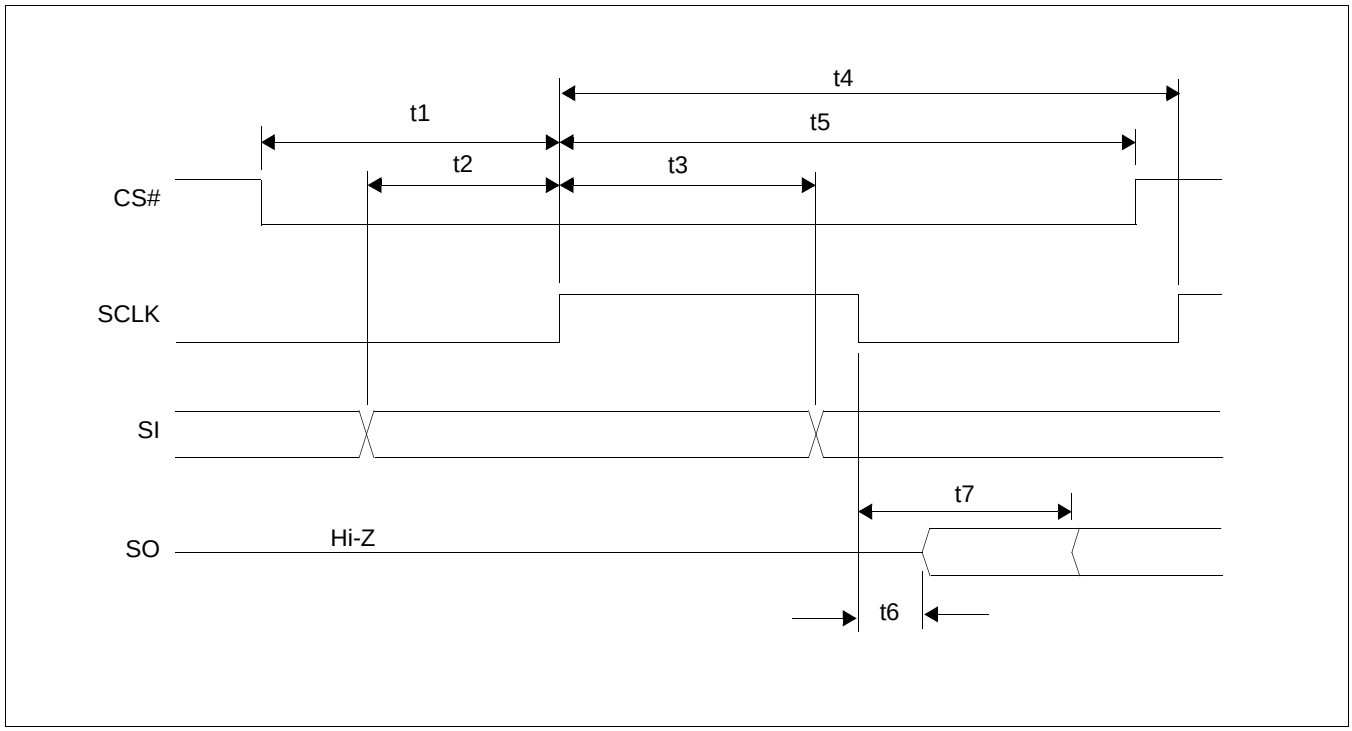


Figure 8-6: 3-Wire Serial Interface Timing

Table 8-6: 3-Wire Serial Interface Timing

Symbol	Parameter	Min	Max	Units
t1	CS# Active to positive edge of SCLK	10	—	ns
t2	SI Setup to positive edge of SCLK	6	—	ns
t3	SI Hold from positive edge of SCLK	8	—	ns
t4	SCLK Period	150	—	ns
t5	Positive edge of SCLK to CS# High	1	—	SCLK
t6	Negative edge of SCLK to SO driven, not Hi-Z	—	22	ns
t7	Negative edge of SCLK to SO Valid Data	—	25	ns

8.4.2 4-Wire Serial Interface (SPI) Timing

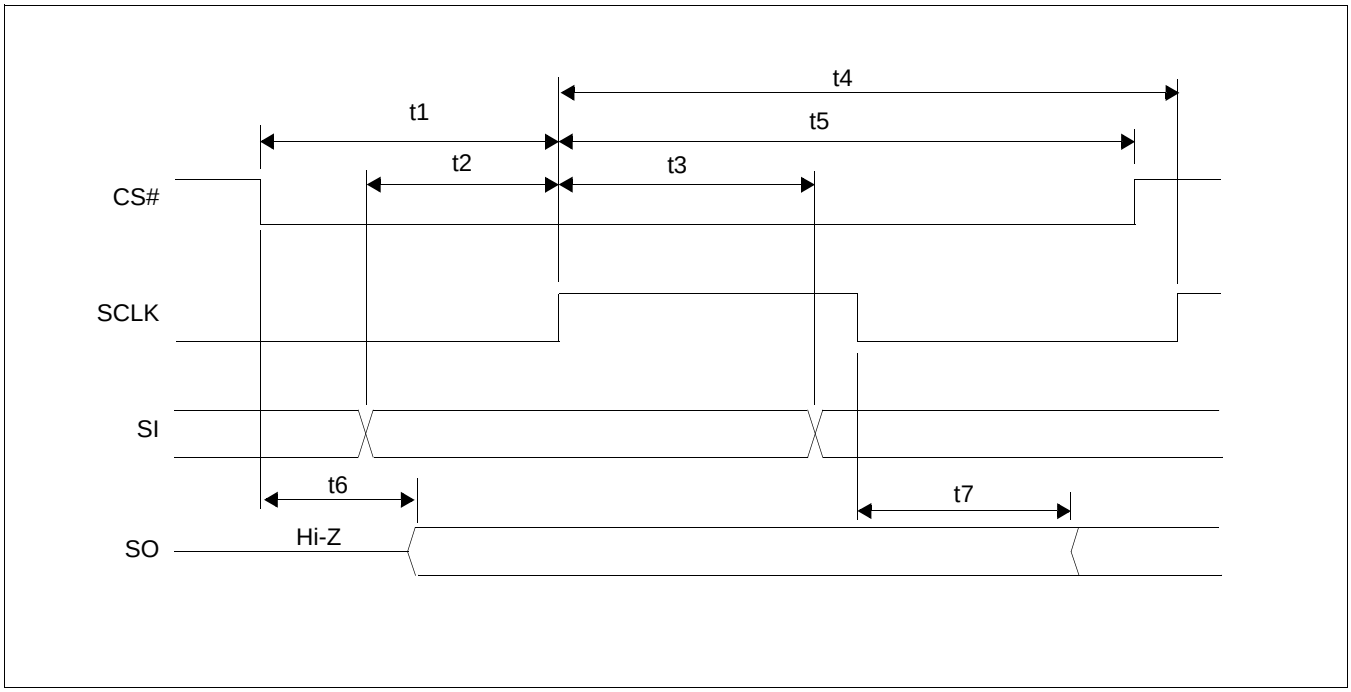


Figure 8-7: 4-Wire Serial Interface (SPI) Timing

Table 8-7: 4-Wire Serial Interface (SPI) Timing

Symbol	Parameter	Min	Max	Units
t1	CS# Active to positive edge of SCLK	10	—	ns
t2	SI Setup to positive edge of SCLK	6	—	ns
t3	SI Hold from positive edge of SCLK	8	—	ns
t4	SCLK Period	100	—	ns
t5	Positive edge of SCLK to CS# high	1	—	SCLK
t6	CS# low to SO driven, not Hi-Z	—	20	ns
t7	Negative edge of SCLK to SO Valid Data	—	25	ns

8.5 Parallel RGB Interface Timing

8.5.1 Vertical Timing

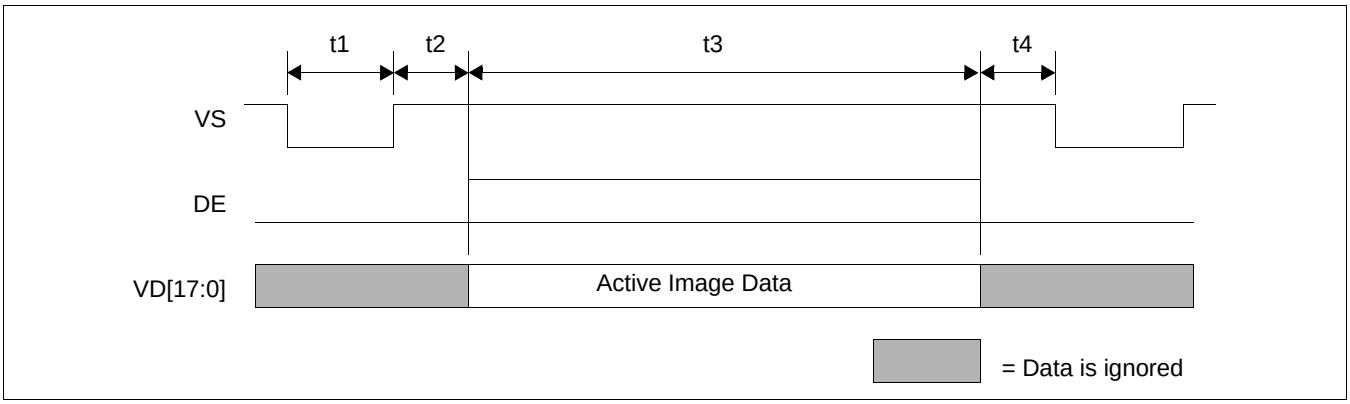


Figure 8-8: Parallel RGB Interface Vertical Timing

Table 8-8: Parallel RGB Interface Vertical Timing

Symbol	Parameter	Min	Max	Units
t1	Vertical Sync Period	2	—	Lines
t2	Vertical Back Porch	2	—	Lines
t3	Vertical Active Frame Period	16	1024	Lines
t4	Vertical Front Porch	2	—	Lines

8.5.2 Horizontal Timing

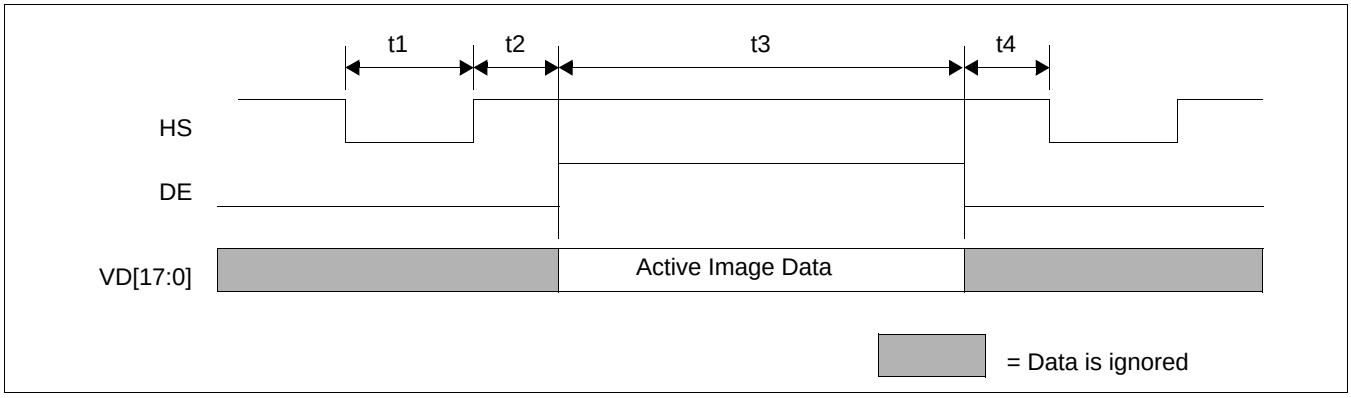


Figure 8-9: Parallel RGB Interface Horizontal Timing

Table 8-9: Parallel RGB Interface Horizontal Timing

Symbol	Parameter	Min	Max	Units
t1	Horizontal Sync Period	2	—	PCLK
t2	Horizontal Back Porch	2	—	PCLK
t3	Horizontal Active Line Period	16	1024	PCLK
t4	Horizontal Front Porch	2	—	PCLK

8.5.3 Input Signal Timings Relative to PCLK

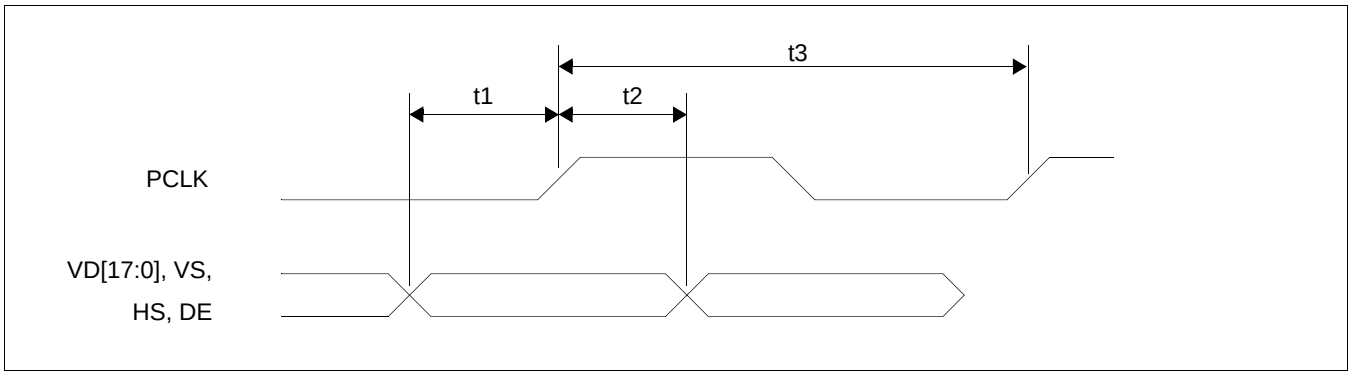


Figure 8-10: Input Signal Timings Relative to PCLK

Table 8-10: Input Signal Timings Relative to PCLK

Symbol	Parameter	Min	Max	Units
t1	VD[17:0], VS, HS, and DE Setup Time	5	—	ns
t2	VD[17:0], VS, HS, and DE Hold Time	8	—	ns
t3	PCLK Period	25	—	ns

8.6 TV Timing

8.6.1 TV Output Timing

The overall PAL and NTSC video timing is shown in Figure 8-11: and Figure 8-12: respectively.

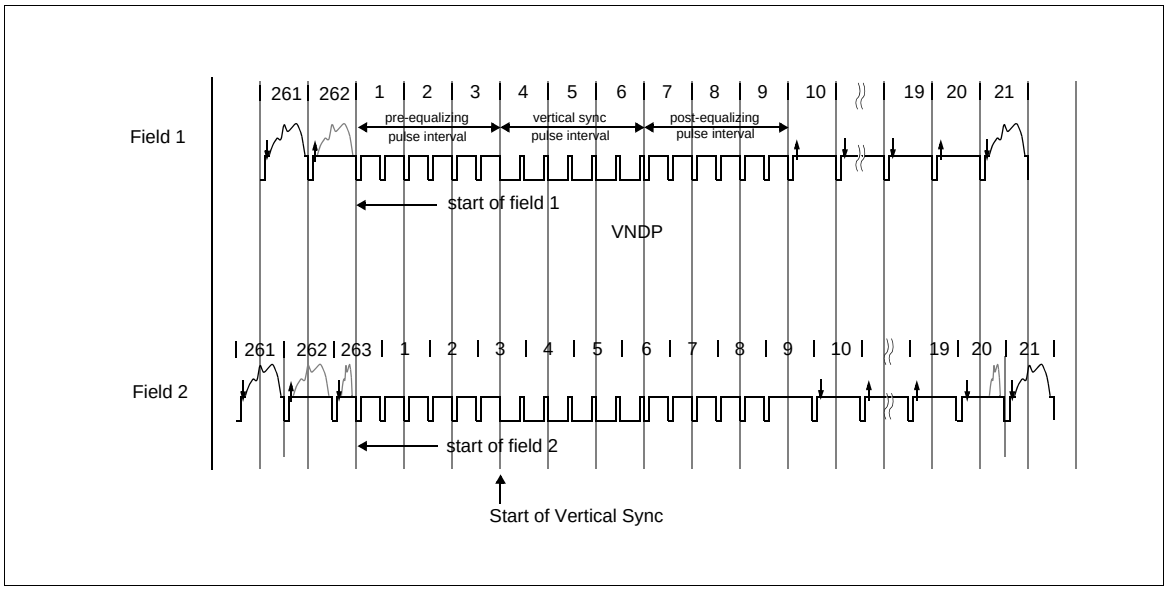


Figure 8-11: NTSC Video Timing

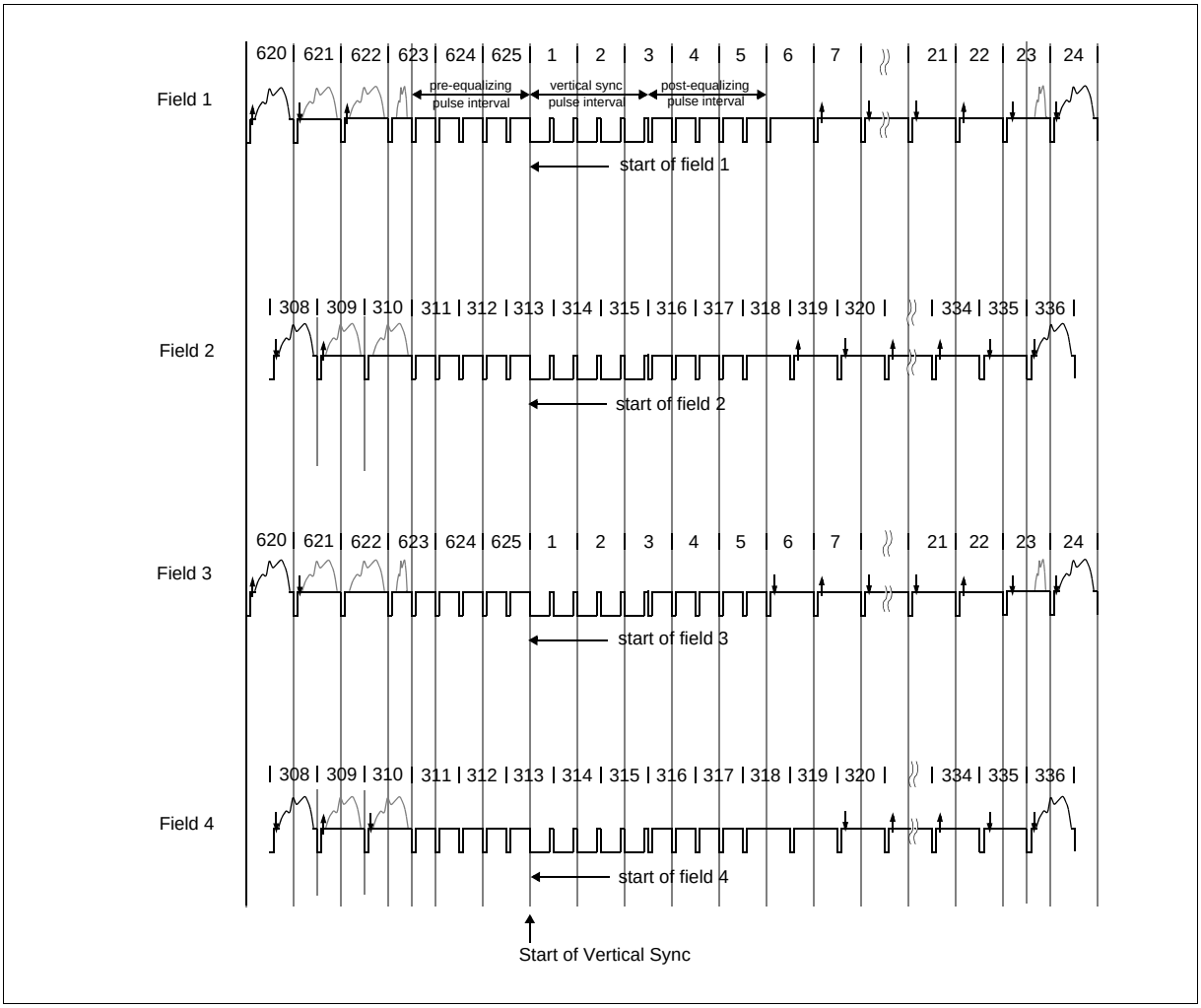


Figure 8-12: PAL Video Timing

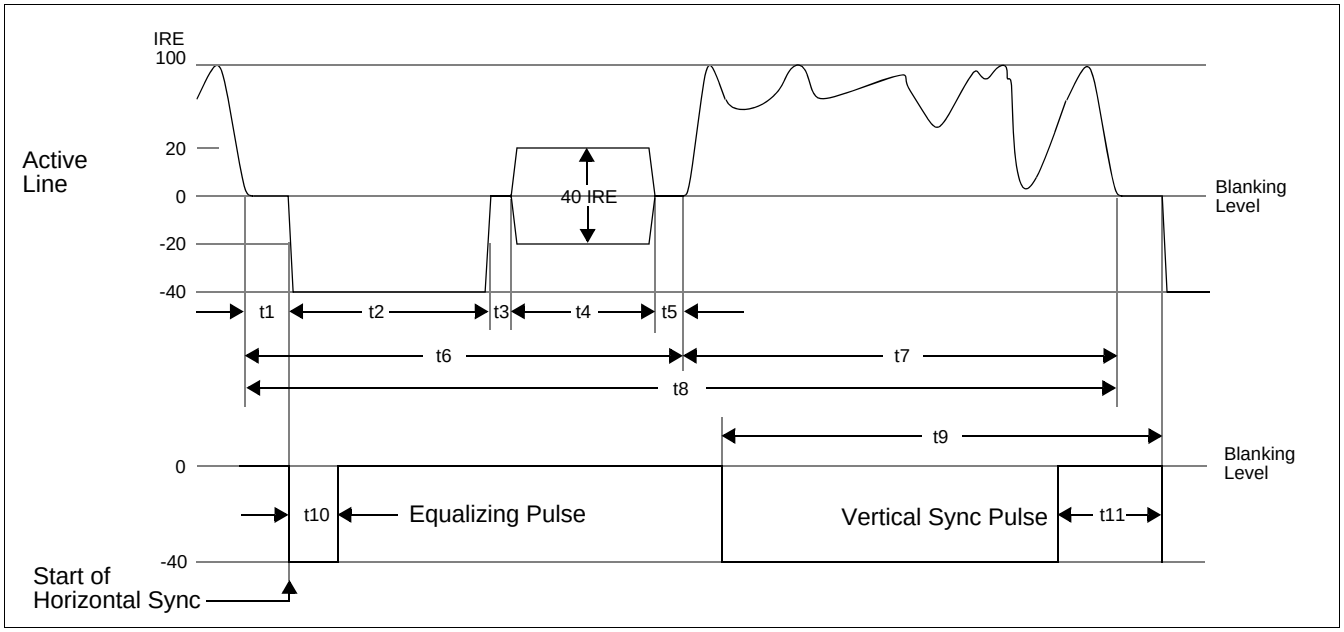


Figure 8-13: Horizontal Timing for NTSC/PAL

Table 8-11: Horizontal Timing for NTSC/PAL

Symbol	Parameter	NTSC M/J (525 Lines)	PAL B/D/G/H/I/N (625 Lines)	PAL Nc (625 Lines)	PAL M (525 Lines)	Units
t1	Front Porch (note 1)	0.96	0.96	0.96	0.96	ps
t2	Horizontal Sync	4.7	4.7	4.7	4.7	ps
t3	Breezeway	0.85	0.9	0.9	1.12	ps
t4	Color Burst	2.52	2.26	2.52	2.52	ps
t5	Color Back Porch (note 2)	1.19	1.85	1.59	0.96	ps
t6	Horizontal Blanking	10.222	10.667	10.667	10.222	ps
t7	Active Video	53.333	53.333	53.333	53.333	ps
t8	Line Period	63.555	64	64	64	ps
t9	Half Line Period	31.7777	32	32	32	ps
t10	Equalizing Pulse	2.3	2.35	2.35	2.35	ps
t11	Vertical Serration	4.66	4.66	4.66	4.66	ps

Note

The values in this table are measured when REG[9Eh] bits 6-4 are set to 000b (default).

1. t1 = 0.074 x (13 ¶ REG[9Eh] bits 6-4) ps (the ¶ is controlled by REG[9Eh] bit 7)
2. t5 = 2.15ps - t1 for NTSC M/J
   = 2.81ps - t1 for PAL B/D/G/H/I/N
   = 2.55ps - t1 for PAL Nc
   = 1.92ps - t1 for PAL M

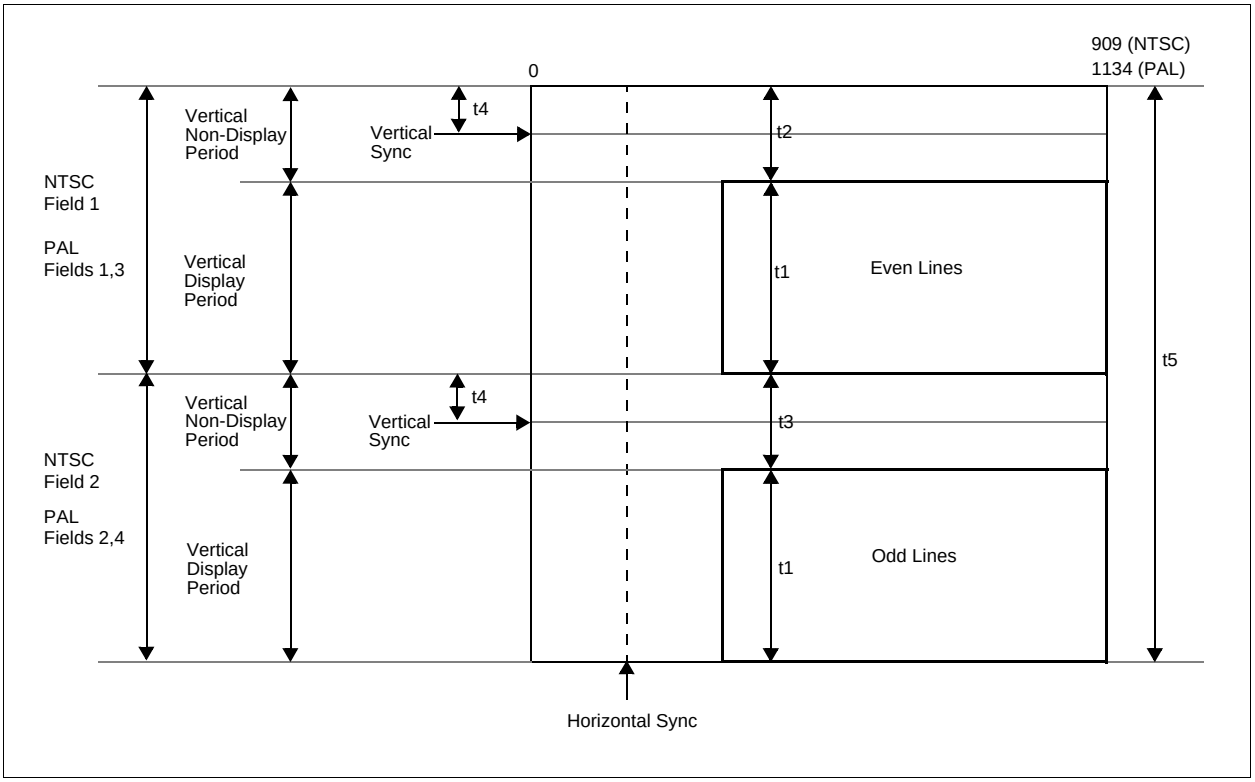


Figure 8-14: Vertical Timing for NTSC/PAL

Table 8-12: Vertical Timing for NTSC/PAL

Symbol	Parameter	NTSC M/J, PAL M	PAL B/D/G/H/I/N/Nc	Units
T_{LINE}	Line Period	63.5555	64	µs
t1	Vertical Field Period	240	288	T_{LINE}
t2	Vertical Even Blanking	22	24	T_{LINE}
t3	Vertical Odd Blanking	23	25	T_{LINE}
t4	Vertical Sync Position (note)	3	3	T_{LINE}
t5	Frame Period	525	625	T_{LINE}

Note

The values in this table are measured when REG[9Eh] bits 3-2 are set to 00b (default).
t4 = 3 - REG[9Eh] bits 3-2

8.6.2 TV Output Parameters

All results in this section are for composite video output.

Luminance Non-Linearity

In a TV system, luminance non-linearity is present if luminance gain is affected by luminance level. In the S1D13746, luminance gain is not affected by the luminance level. The luminance non-linearity is only affected by rounding accuracy of the circuit and DAC performance. These numbers are calculated by comparing the amplitudes of the individual steps in the 10-Step Staircase test pattern with the worst case DAC parameters taken into account. The difference between the largest steps and smallest steps, expressed as a percentage of the largest step amplitude, is the amount of luminance non-linearity distortion.

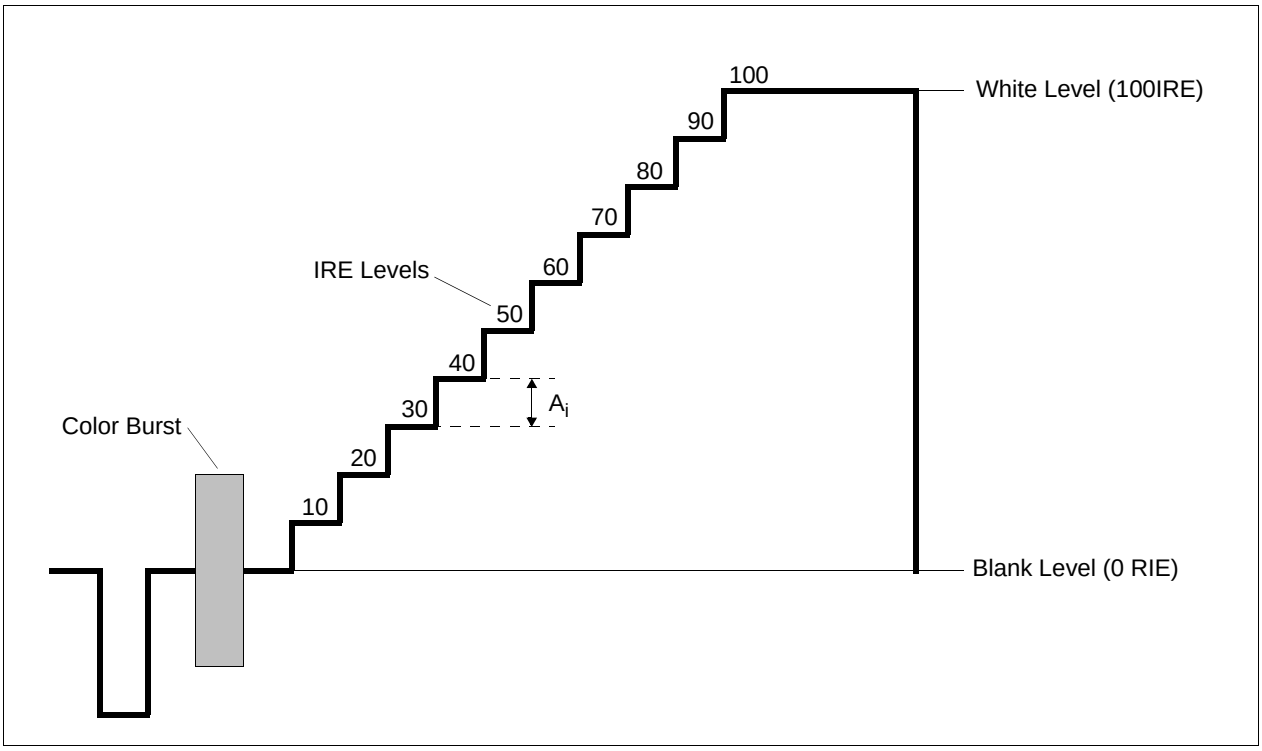


Figure 8-15: Luminance Non-Linearity

Luminance Non-Linearity = $[Max(A_i) - Min(A_i)] \div Max(A_i)$
where i = position of step from 1 to 10

Table 8-13: Luminance Non-Linearity (Using 10-Step Staircase)

	PAL				NTSC	
	B,D,G,H,I	**M**	**N**	**Nc**	**M**	**J**
Typical	7.14%	0.00%	0.00%	7.14%	0.00%	6.67%
Worst Case	41.18%	37.50%	37.50%	41.18%	37.50%	38.89%

75% and 100% Color Bar Levels

These numbers are calculated based on 75% and 100% Color Bar test patterns with the worst case DAC parameters taken into account.

Table 8-14: 75% and 100% Color Bar Levels

			75% Color Bar (mV)						100% Color Bar (mV)					
			PAL				NTSC		PAL				NTSC	
			B,D,G, H,I	M	N	Nc	M	J	B,D,G, H,I	M	N	Nc	M	J
Sync Tip		Max	30.75	30.75	30.75	30.75	30.75	30.75	30.75	30.75	30.75	30.75	30.75	30.75
		Typ	20.33	20.33	20.33	20.33	20.33	20.33	20.33	20.33	20.33	20.33	20.33	20.33
		Min	11.44	11.44	11.44	11.44	11.44	11.44	11.44	11.44	11.44	11.44	11.44	11.44
Blank		Max	360.65	343.87	343.87	360.65	343.87	343.87	360.65	343.87	343.87	360.65	343.87	343.87
		Typ	320.23	304.99	304.99	320.23	304.99	304.99	320.23	304.99	304.99	320.23	304.99	304.99
		Min	281.35	267.62	267.62	281.35	267.62	267.62	281.35	267.62	267.62	281.35	267.62	267.62
Color Burst	High Tip	Max	522.80	506.02	506.02	522.80	499.03	499.03	522.80	506.02	506.02	522.80	499.03	499.03
		Typ	467.64	452.39	452.39	467.64	446.04	446.04	467.64	452.39	452.39	467.64	446.04	446.04
		Min	414.02	400.29	400.29	414.02	394.57	394.57	414.02	400.29	400.29	414.02	394.57	394.57
	Low Tip	Max	197.10	180.32	180.32	197.10	187.31	187.31	197.10	180.32	180.32	197.10	187.31	187.31
		Typ	171.55	156.30	156.30	171.55	162.66	162.66	171.55	156.30	156.30	171.55	162.66	162.66
		Min	147.54	133.81	133.81	147.54	139.53	139.53	147.54	133.81	133.81	147.54	139.53	139.53
White		Max	936.56	944.95	944.95	936.56	944.95	930.97	1126.67	1129.46	1129.46	1126.67	1129.46	1126.67
		Typ	843.79	851.42	851.42	843.79	851.42	838.71	1016.62	1019.16	1019.16	1016.62	1019.16	1016.62
		Min	752.55	759.41	759.41	752.55	759.41	747.98	908.09	910.38	910.38	908.09	910.38	908.09
Yellow	High Tip	Max	1128.06	1123.87	1123.87	1128.06	1123.87	1126.67	1375.48	1365.70	1365.70	1375.48	1365.70	1385.27
		Typ	1017.89	1014.08	1014.08	1017.89	1014.08	1016.62	1242.82	1233.92	1233.92	1242.82	1233.92	1251.71
		Min	909.24	905.81	905.81	909.24	905.81	908.09	1111.67	1103.67	1103.67	1111.67	1103.67	1119.68
	Low Tip	Max	610.86	641.61	641.61	610.86	641.61	599.68	697.53	724.09	724.09	697.53	724.09	687.74
		Typ	547.70	575.66	575.66	547.70	575.66	537.54	626.49	650.64	650.64	626.49	650.64	617.60
		Min	486.07	511.23	511.23	486.07	511.23	476.92	556.98	578.71	578.71	556.98	578.71	548.97
Cyan	High Tip	Max	1123.87	1126.67	1125.27	1123.87	1126.67	1123.87	1378.28	1369.89	1369.89	1378.28	1369.89	1385.27
		Typ	1014.08	1016.62	1015.35	1014.08	1016.62	1014.08	1245.36	1237.73	1237.73	1245.36	1237.73	1251.71
		Min	905.81	908.09	906.95	905.81	908.09	905.81	1113.96	1107.10	1107.10	1113.96	1107.10	1119.68
	Low Tip	Max	401.18	438.92	438.92	401.18	438.92	378.82	415.16	451.51	451.51	415.16	451.51	396.99
		Typ	357.09	391.40	391.40	357.09	391.40	336.75	369.79	402.83	402.83	369.79	402.83	353.27
		Min	314.52	345.40	345.40	314.52	345.40	296.22	325.95	355.69	355.69	325.95	355.69	311.09
Green	High Tip	Max	1035.81	1040.00	1040.00	1035.81	1040.00	1031.61	1265.05	1253.87	1253.87	1265.05	1253.87	1260.86
		Typ	934.02	937.83	937.83	934.02	937.83	930.21	1142.42	1132.26	1132.26	1142.42	1132.26	1138.61
		Min	833.75	837.18	837.18	833.75	837.18	830.32	1021.32	1012.17	1012.17	1021.32	1012.17	1017.89
	Low Tip	Max	355.05	401.18	401.18	355.05	401.18	336.88	360.65	399.78	399.78	360.65	399.78	342.47
		Typ	315.15	357.09	357.09	315.15	357.09	298.63	320.23	355.82	355.82	320.23	355.82	303.71
		Min	276.77	314.52	314.52	276.77	314.52	261.91	281.35	313.37	313.37	281.35	313.37	266.48
Magenta	High Tip	Max	940.75	944.95	944.95	940.75	944.95	930.97	1125.27	1125.27	1125.27	1125.27	1125.27	1121.08
		Typ	847.61	851.42	851.42	847.61	851.42	838.71	1015.35	1015.35	1015.35	1015.35	1015.35	1011.53
		Min	755.98	759.41	759.41	755.98	759.41	747.98	906.95	906.95	906.95	906.95	906.95	903.52
	Low Tip	Max	260.00	306.13	306.13	260.00	306.13	236.24	220.86	271.18	271.18	220.86	271.18	202.69
		Typ	228.74	270.67	270.67	228.74	270.67	207.14	193.16	238.91	238.91	193.16	238.91	176.64
		Min	199.00	236.74	236.74	199.00	236.74	179.56	166.98	208.15	208.15	166.98	208.15	152.11
Red	High Tip	Max	894.62	907.20	907.20	894.62	907.20	889.03	1070.75	1072.15	1073.55	1070.75	1073.55	1072.15
		Typ	805.67	817.11	817.11	805.67	817.11	800.59	965.79	967.06	968.33	965.79	968.33	967.06
		Min	718.24	728.53	728.53	718.24	728.53	713.67	862.35	863.49	864.63	862.35	864.63	863.49
	Low Tip	Max	171.94	219.46	220.86	171.94	220.86	143.98	107.63	155.16	155.16	107.63	155.16	83.87
		Typ	148.68	191.89	193.16	148.68	193.16	123.26	90.22	133.43	133.43	90.22	133.43	68.62
		Min	126.95	165.84	166.98	126.95	166.98	104.08	74.34	113.23	113.23	74.34	113.23	54.90

Table 8-14: 75% and 100% Color Bar Levels (Continued)

			75% Color Bar (mV)						100% Color Bar (mV)					
			PAL				NTSC		PAL				NTSC	
			B,D,G, H,I	M	N	Nc	M	J	B,D,G, H,I	M	N	Nc	M	J
Blue	High Tip	Max	684.95	704.52	704.52	684.95	704.52	673.76	792.58	806.56	806.56	792.58	806.56	781.40
		Typ	615.05	632.84	632.84	615.05	632.84	604.89	712.90	725.61	725.61	712.90	725.61	702.74
		Min	546.69	562.70	562.70	546.69	562.70	537.54	634.75	646.19	646.19	634.75	646.19	625.60
	Low Tip	Max	169.14	222.26	222.26	169.14	222.26	146.77	106.24	164.95	164.95	106.24	164.95	83.87
		Typ	146.14	194.43	194.43	146.14	194.43	125.81	88.95	142.33	142.33	88.95	142.33	68.62
		Min	124.66	168.12	168.12	124.66	168.12	106.36	73.20	121.23	121.23	73.20	121.23	54.90
Black		Max	360.65	402.58	402.58	360.65	402.58	343.87	360.65	402.58	402.58	360.65	402.58	343.87
		Typ	320.23	358.36	358.36	320.23	358.36	304.99	320.23	358.36	358.36	320.23	358.36	304.99
		Min	281.35	315.66	315.66	281.35	315.66	267.62	281.35	315.66	315.66	281.35	315.66	267.62

10-Step Staircase Levels

These numbers are calculated based on 10-Step Staircase test patterns with the worst case DAC parameters taken into account.

Table 8-15: 10-Step Staircase Levels

			PAL				NTSC		Units
			B,D,G,H,I	M	N	Nc	M	J	
Step	1st	Max	438.92	475.27	475.27	438.92	475.27	422.15	mV
		Typ	391.40	424.44	424.44	391.40	424.44	376.15	mV
		Min	345.40	375.13	375.13	345.40	375.13	331.67	mV
	2nd	Max	517.20	547.96	547.96	517.20	547.96	500.43	mV
		Typ	462.56	490.52	490.52	462.56	490.52	447.31	mV
		Min	409.44	434.60	434.60	409.44	434.60	395.72	mV
	3rd	Max	589.89	620.65	620.65	589.89	620.65	578.71	mV
		Typ	528.64	556.60	556.60	528.64	556.60	518.48	mV
		Min	468.91	494.08	494.08	468.91	494.08	459.77	mV
	4th	Max	668.17	693.33	693.33	668.17	693.33	656.99	mV
		Typ	599.80	622.68	622.68	599.80	622.68	589.64	mV
		Min	532.96	553.55	553.55	532.96	553.55	523.81	mV
	5th	Max	746.45	766.02	766.02	746.45	766.02	735.27	mV
		Typ	670.97	688.76	688.76	670.97	688.76	660.80	mV
		Min	597.01	613.02	613.02	597.01	613.02	587.86	mV
	6th	Max	824.73	838.71	838.71	824.73	838.71	813.55	mV
		Typ	742.13	754.84	754.84	742.13	754.84	731.96	mV
		Min	661.06	672.49	672.49	661.06	672.49	651.91	mV
	7th	Max	897.42	911.40	911.40	897.42	911.40	891.83	mV
		Typ	808.21	820.92	820.92	808.21	820.92	803.13	mV
		Min	720.53	731.96	731.96	720.53	731.96	715.95	mV
	8th	Max	975.70	984.09	984.09	975.70	984.09	970.11	mV
		Typ	879.37	887.00	887.00	879.37	887.00	874.29	mV
		Min	784.57	791.44	791.44	784.57	791.44	780.00	mV
	9th	Max	1053.98	1056.77	1056.77	1053.98	1056.77	1048.39	mV
		Typ	950.54	953.08	953.08	950.54	953.08	945.45	mV
		Min	848.62	850.91	850.91	848.62	850.91	844.05	mV
	10th	Max	1132.26	1129.46	1129.46	1132.26	1129.46	1132.26	mV
		Typ	1021.70	1019.16	1019.16	1021.70	1019.16	1021.70	mV
		Min	912.67	910.38	910.38	912.67	910.38	912.67	mV

Frequency Response

In a TV system, frequency response measurements evaluate a system's ability to uniformly transfer signal components of different frequencies without affecting their amplitudes. This parameter, which is also known as gain/frequency distortion or amplitude versus frequency response, evaluates the system's amplitude response over the entire video spectrum. In the S1D13746, the TV function is operating at 26-27MHz, which is over the video spectrum with enough margins such that TV signal amplitude will not be affected by the frequency within the video spectrum. Frequency response measurement is only affected by the rounding accuracy of the circuit and DAC performance. These numbers are calculated by comparing the amplitudes of the Mutliburst test patterns (this test pattern is not enabled in the S1D13746, so calculation is only based on simulation) with the worst case DAC parameters taken into account. The amplitude of each frequency packets is compared with that of the lowest frequency packet, and expressed in dB.

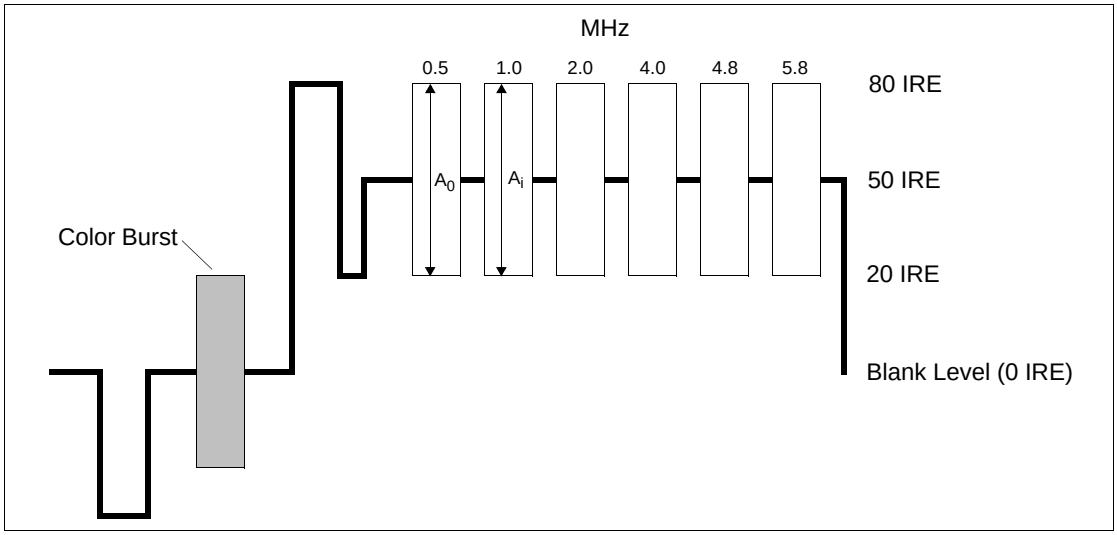


Figure 8-16: Frequency Response

Frequency Response = $20 \times \log(A_i \div A_0)$

where

A_0 = amplitude of 0.5MHz burst

A_i = amplitude of burst above 0.5MHz, i = 1 to 5

Table 8-16: Frequency Response

			Frequency Response (in dB)					
			PAL				NTSC	
			B,D,G,H,I	M	N	Nc	M	J
Burst Frequency	1MHz	Max	0.64	0.75	0.64	0.64	0.75	0.75
		Typ	0.00	0.00	0.00	0.00	0.00	0.00
		Min	-0.64	-0.75	-0.64	-0.64	-0.75	-0.75
	2MHz	Max	0.64	0.75	0.64	0.64	0.75	0.75
		Typ	0.00	0.00	0.00	0.00	0.00	0.00
		Min	-0.64	-0.75	-0.64	-0.64	-0.75	-0.75
	3MHz (4MHz)	Max	0.64	0.63	0.64	0.53	0.63	0.63
		Typ	0.00	-0.13	0.00	-0.11	-0.13	-0.13
		Min	-0.64	-0.88	-0.64	-0.75	-0.88	-0.88
	3.58MHz (4.8MHz)	Max	0.64	0.75	0.64	0.64	0.75	0.75
		Typ	0.00	0.00	0.00	0.00	0.00	0.00
		Min	-0.64	-0.75	-0.64	-0.64	-0.75	-0.75
	4.2MHz (5.8MHz)	Max	0.64	0.75	0.64	0.64	0.75	0.75
		Typ	0.00	0.00	0.00	0.00	0.00	0.00
		Min	-0.64	-0.75	-0.64	-0.64	-0.75	-0.75

Chrominance Gain Non-Linearity

In a TV system, chrominance non-linearity gain distortion is present if chrominance gain is dependent on chrominance amplitude. In the S1D13746, the chrominance gain is not affected by the chrominance amplitude. The chrominance gain non-linearity is only affected by rounding accuracy of the circuit and DAC performance. These numbers are calculated by comparing the amplitude of packets in the Modulated Pedestal test pattern (this test pattern is not enabled in the S1D13746, so calculation is only based on simulation) with the worst case DAC parameters taken into account. The amplitude of the packets compared with the amplitude of the normalized middle packet, expressed as percentage of the nominal amplitude is the chrominance gain non-linearity.

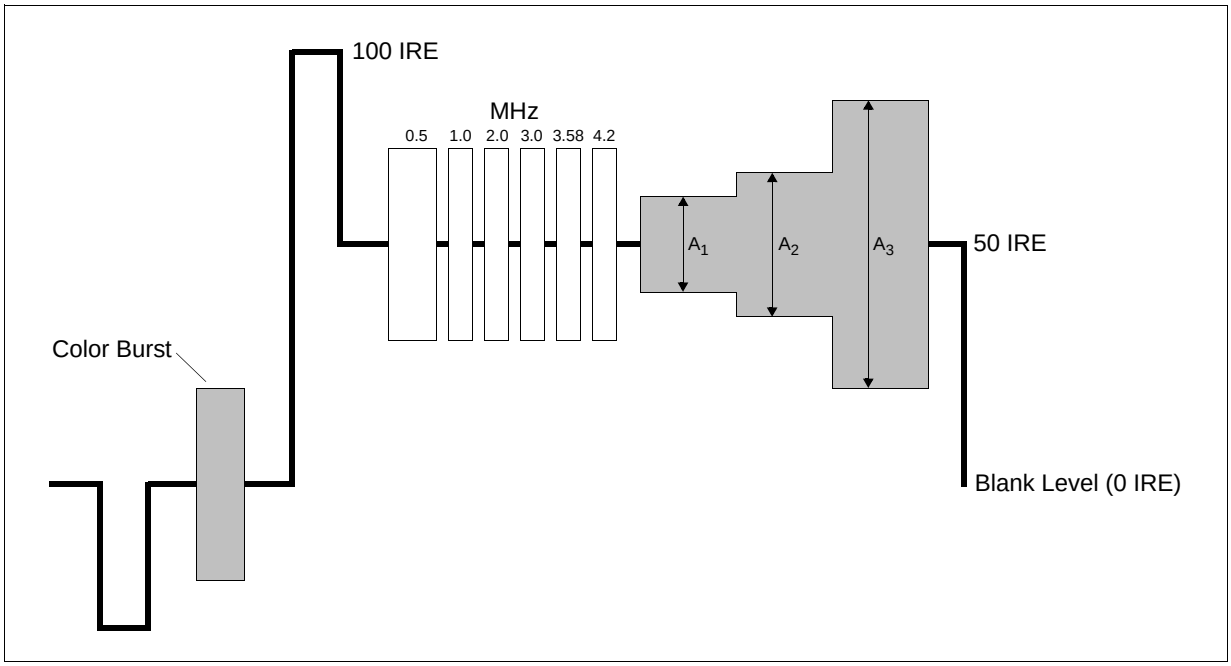


Figure 8-17: Chrominance Gain Non-Linearity

Chrominance Gain Non-Linearity = $100 \times | (A_i - k_i \times A_2) \div (k_i \times A_2) |$

where:

A = amplitude of received sub-carrier

i = position of burst (1 being the smallest, 3 the largest)

$k_i = (2i - 1) \div 3$ for 625-line signal

$k_i = 2^{i-2}$ for 525-line signal

Table 8-17: Chrominance Gain Non-Linearity

			PAL				NTSC	
			B,D,G,H,I	M	N	Nc	M	J
Chrominance Gain Non-Linearity	Smallest Pedestal	Max	15.24%	16.59%	15.24%	15.24%	16.59%	16.59%
		Typ	0.00%	0.45%	0.00%	0.00%	0.45%	0.45%
		Min	-14.16%	-15.74%	-14.16%	-14.16%	-15.74%	-15.74%
	Largest Pedestal	Max	6.48%	8.77%	6.48%	6.48%	8.77%	8.77%
		Typ	0.37%	0.22%	0.37%	0.37%	0.22%	0.22%
		Min	-5.31%	-7.45%	-5.31%	-5.31%	-7.45%	-7.45%

Chrominance-to-Luminance Intermodulation

In a TV system, chrominance-to-luminance intermodulation is present when luminance amplitude is affected by superimposed chrominance. In the S1D13746, the luminance and chrominance are processed independently and combined only before going to the DAC. The luminance amplitude is not affected by the chrominance, the chrominance-to-luminance is only affected by the rounding accuracy of the circuit and DAC performance. These numbers are calculated by comparing the averaged level of the packets in the Modulated Pedestal test pattern (this test pattern is not enabled in the S1D13746, so calculation is only based on simulation) with the worst case DAC parameters taken into account. The averaged level (high tip and low tip levels) of each packet is compared with the level of luminance only portion of the signal, and expressed in percentage.

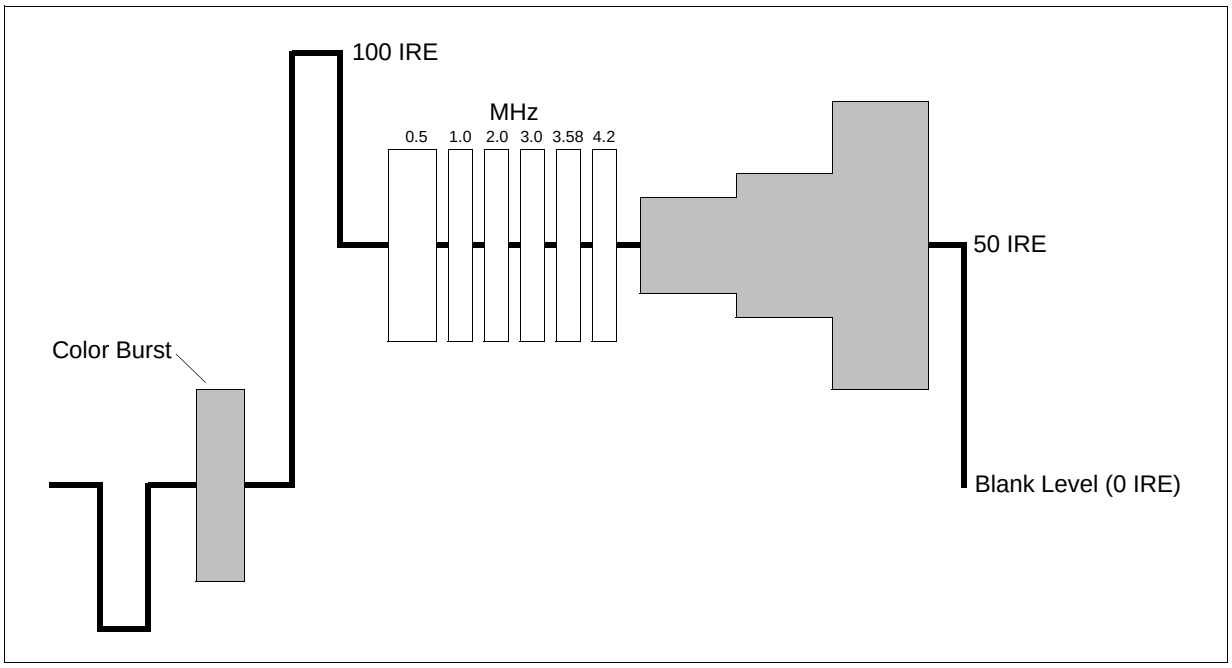


Figure 8-18: Before Chrominance is Filtered

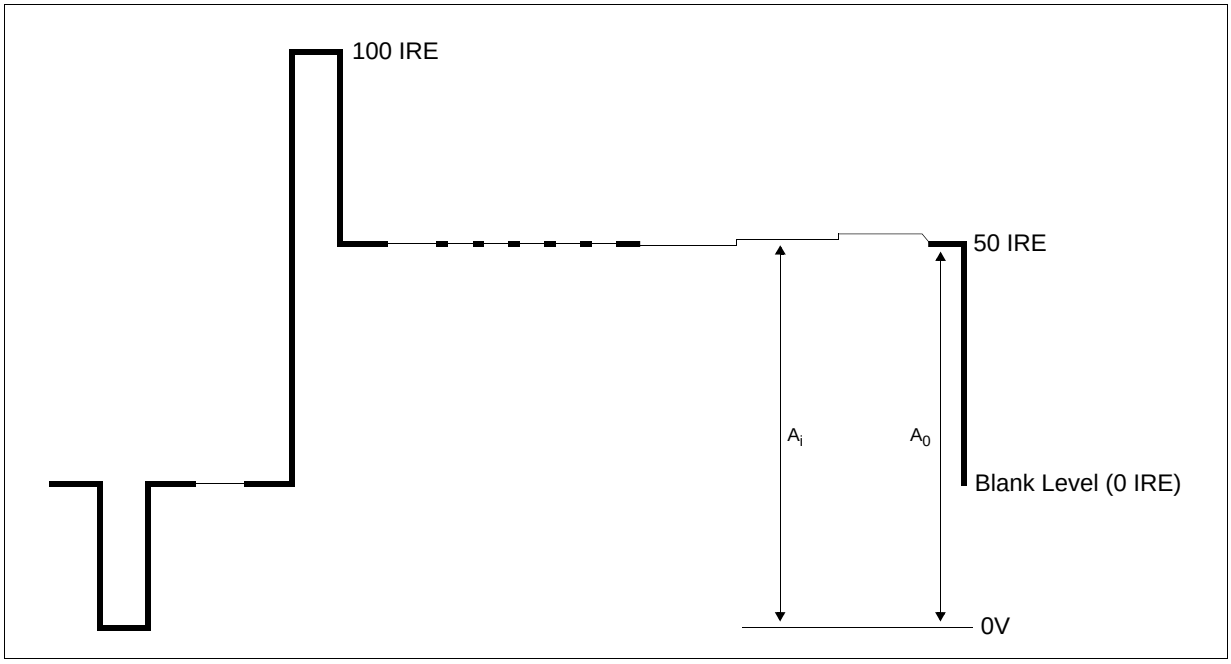


Figure 8-19: After Chrominance is Filtered

Chrominance-to-Luminance Intermodulation = 100 * (A_i - A_0) ‰ A0

where:

A = amplitude of received sub-carrier.

i = position of burst (1 being the smallest, 2 the middle, 3 the largest).

A_0 = amplitude of luminance only.

Table 8-18: Chrominance to Luminance Intermodulation

			PAL				NTSC	
			B,D,G,H,I	M	N	Nc	M	J
Inter-Modulation	Smallest Pedestal	Max	2.21%	2.24%	2.21%	2.21%	2.24%	2.24%
		Typ	-0.10%	-0.10%	-0.10%	-0.10%	-0.10%	-0.10%
		Min	-2.35%	-2.38%	-2.35%	-2.35%	-2.38%	-2.38%
	Middle Pedestal	Max	2.21%	2.24%	2.21%	2.21%	2.24%	2.24%
		Typ	-0.10%	-0.10%	-0.10%	-0.10%	-0.10%	-0.10%
		Min	-2.35%	-2.38%	-2.35%	-2.35%	-2.38%	-2.38%
	Largest Pedestal	Max	2.21%	2.24%	2.21%	2.21%	2.24%	2.24%
		Typ	-0.10%	-0.10%	-0.10%	-0.10%	-0.10%	-0.10%
		Min	-2.35%	-2.38%	-2.35%	-2.35%	-2.38%	-2.38%

Differential Gain Non-Linearity

In a TV system, differential gain non-linearity is present if chrominance gain is dependent on luminance level. These amplutide errors are a result of the system's inability to uniformly process the high-frequency chrominance signal at all luminance levels. In the S1D13746, the luminance and chrominance are processed independently and combined only before going to the DAC. The chrominance gain is not affected by the luminance level,

the differential gain non-linearity is only affected by DAC performance. These numbers are calculated by comparing the peak-to-peak chrominance amplitude of the steps in the Modulated 10-Step Staircase test pattern with the worst case DAC parameters taken into account. Differential gain non-linearity is maximum, minimum, and peak deviation chrominance amplitude of all 10 steps, compared with the chrominance amplitude at the blanking (black) level, and expressed in percentage.

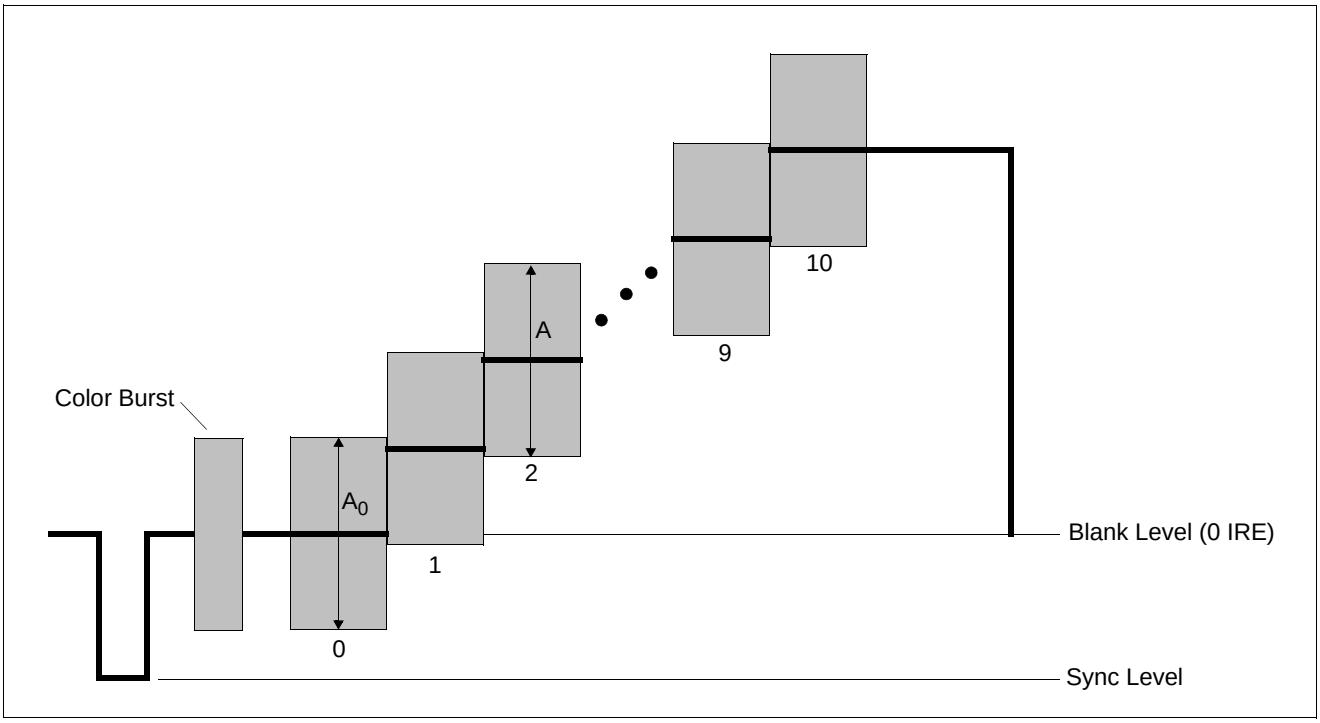


Figure 8-20: Differential Gain Non-Linearity

Differential Gain Non-Linearity:

$+X = 100 \times | Max(A_i) \div A_0 - 1 |$

$-Y = 100 \times | Min(A_i) \div A_0 - 1 |$

$X+Y = 100 \times | (Max(A_i) - Min(A_i)) \div A_0 |$

where:

A_0 = amplitude of the received sub-carrier at blanking level.

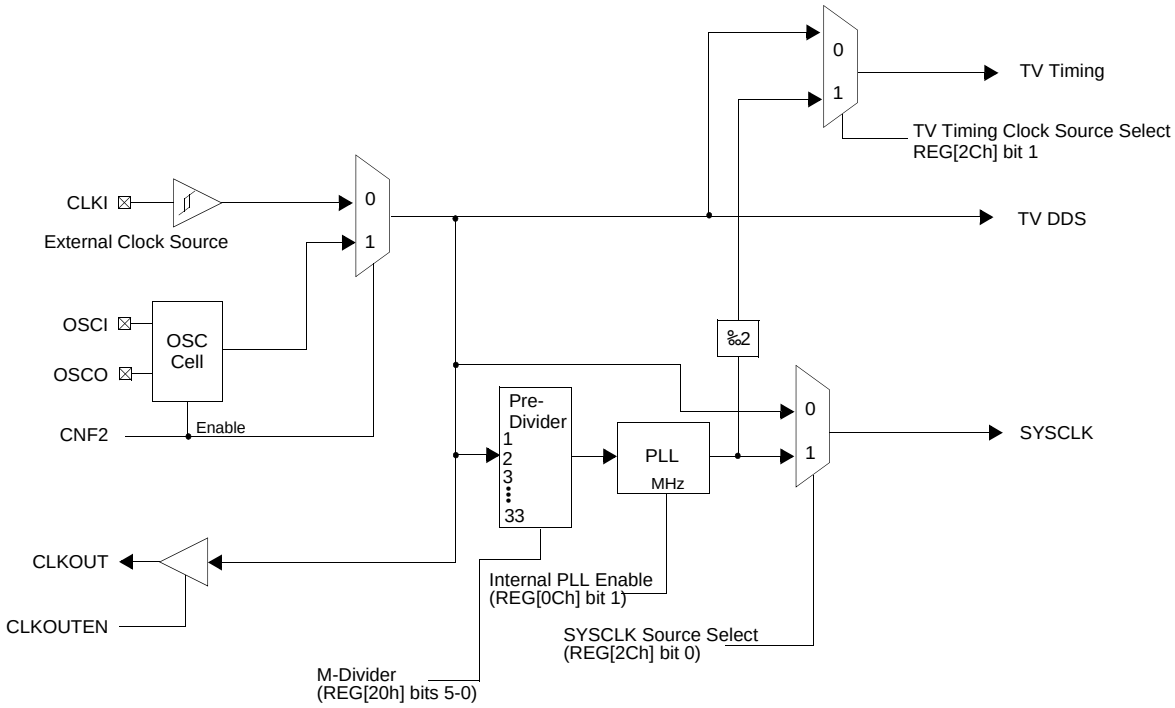
A_i = amplitude of the sub-carrier on any relevant tread of the staircase, i = 1 to 10

Table 8-19: Differential Gain Non-Linearity

			PAL				NTSC	
			B,D,G,H,I	M	N	Nc	M	J
Differential Gain Non-Linearity	+X	Worst Case	10.67%	11.27%	11.27%	10.67%	11.37%	11.37%
		Typical	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
	-Y	Worst Case	9.64%	10.13%	10.13%	9.64%	10.21%	10.21%
		Typical	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
	X+Y	Worst Case	10.67%	11.27%	11.27%	10.67%	11.37%	11.37%
		Typical	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%

9 Clocks

9.1 Clock Block Diagram



TV DDS = clock source for TV Direct Digital Synthesis (DDS) of the sub-carrier.
TV Timing = clock source for TV timing circuits.

Note:
The TV Clock Setting bits (REG[4Eh] bits 5-4) need to be programmed to reflect the CLKI frequency used.
See Section 11.3.3, “TV Configuration Registers” on page 71

Figure 9-1: S1D13746 Clock Block Diagram

9.2 PLL Block Diagram

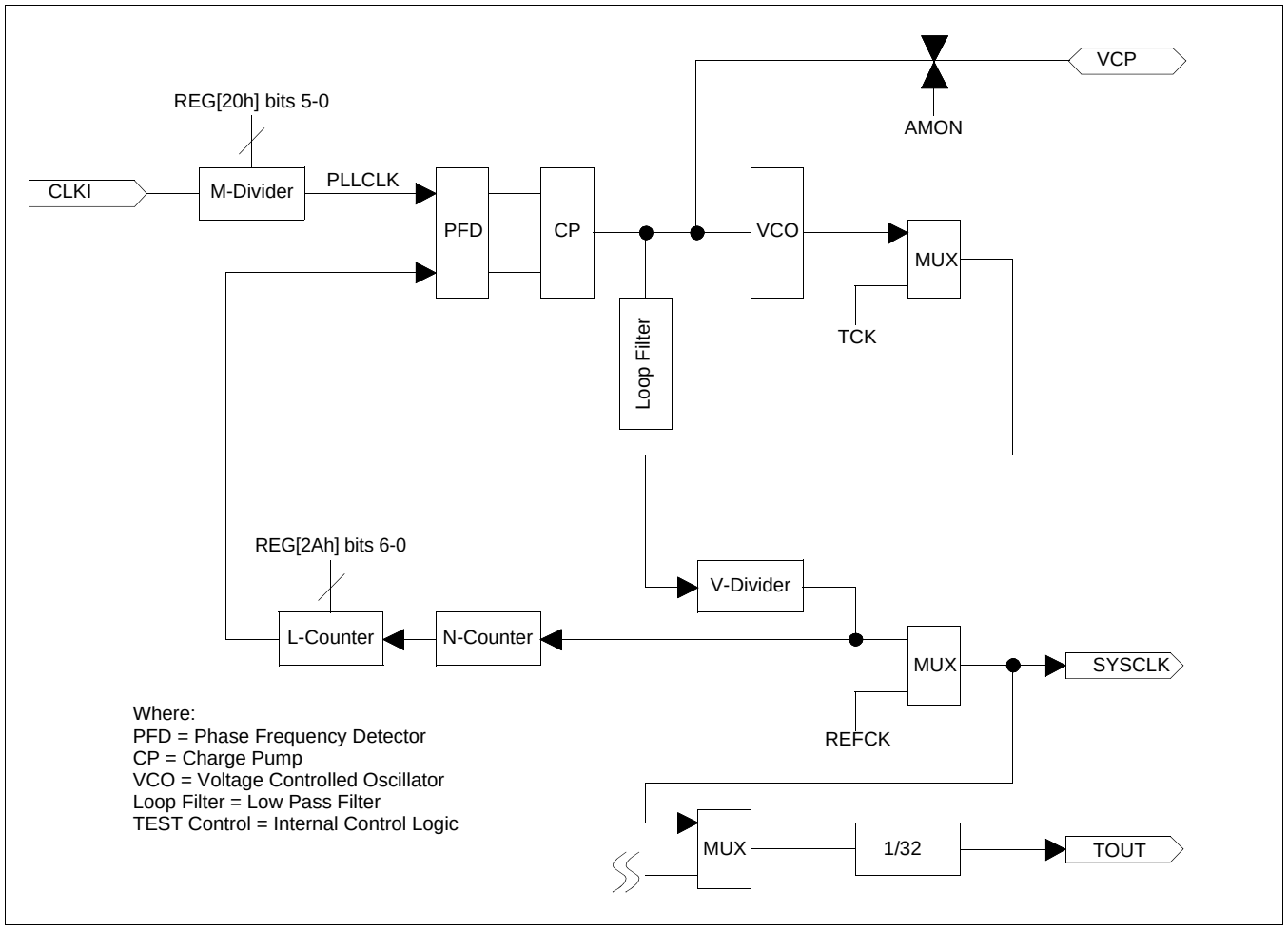


Figure 9-2: PLL Block Diagram

10 Memory Map

The S1D13746 includes 312k byte of embedded SRAM. The memory is used for the Display Buffer which contains both main image data and overlay image data.

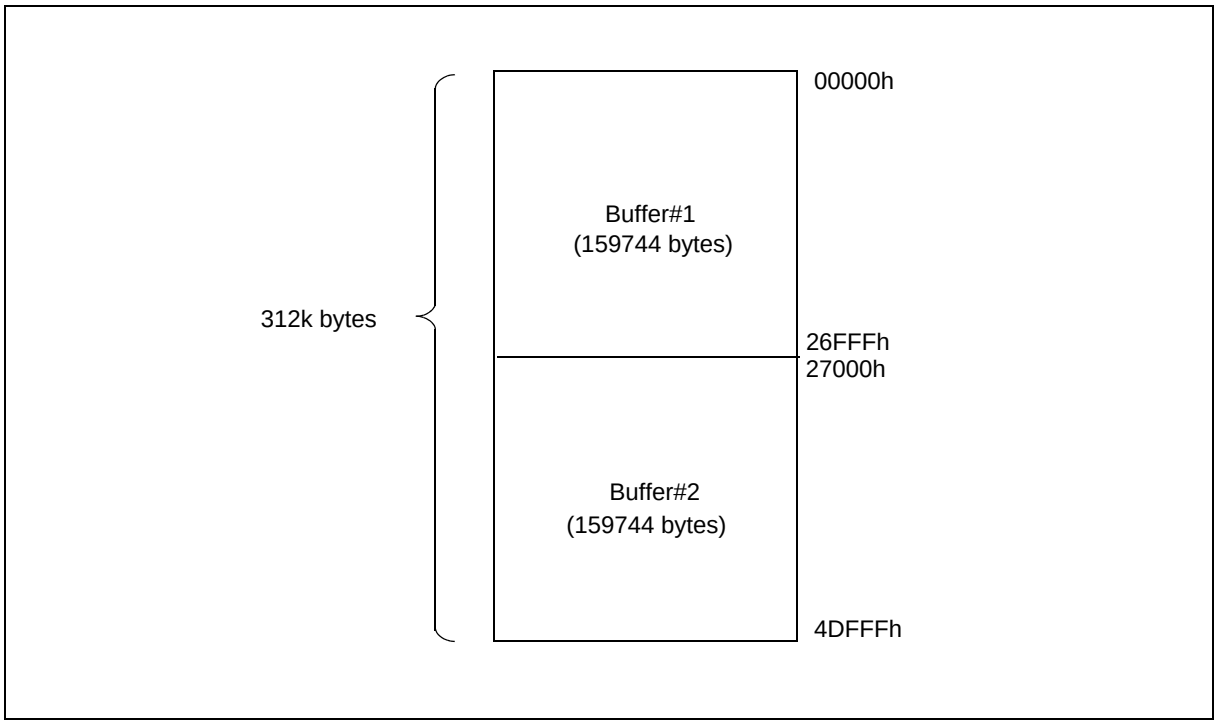


Figure 10-1: Physical Memory

11 Registers

This section discusses how and where to access the S1D13746 registers. It also provides detailed information about the layout and usage of each register.

All S1D13746 registers are accessed through either the Intel 80 interface or the Serial Interface. All register access is 8-bit only, except for the Display Memory Data Port (REG[A0h]), which is accessed as 16-bit (if CNF1=1) or 8-bit (if CNF1=0). The width of the Intel 80 interface is configured by the configuration pins (CNF).

Burst data reads/writes from/to the register space are supported. A write with D/C# low sets up the register address for the next register read/write. The register address increments on a word boundary after each read or write with D/C# high. This applies to all register write accesses except the Memory Data Port (REG[A0h]), the TV Filter Coefficient and User Clock Ratio Data register (REG[56h]). All writes to these registers auto increment the internal memory address only.

11.1 Register Mapping

The S1D13746 registers are memory-mapped. Asynchronous registers are accessible at all times. Synchronous registers are only accessible when power save mode is disabled (REG[2Eh]) and the PLL is locked (REG[20h] bit 7 = 1b).

Table 11-1: S1D13746 Register Mapping

Address	Type	Function
00h to 02h	Asynchronous	Product Information Registers
20h to 2Eh	Asynchronous	Clock Configuration Registers
40h to 56h	Synchronous	TV Configuration Registers
60h to 6Ah	Synchronous	Input Data Control Registers
80h to 9Ch	Synchronous	Display Output Control Registers
A0h to A6h	Synchronous	Display Memory Access Registers
C0h to EAh	Synchronous	3X3 Pixel Matrix Filter Registers
ECh to EEh	Synchronous	Miscellaneous Registers
F0h to FAh	Asynchronous	General Purpose IO Pins Registers

11.2 Register Set

The S1D13746 registers are listed in the following table.

Table 11-2: S1D13746 Register Set

Register	Pg	Register	Pg
Product Information Registers			
REG[00h] Revision Code Register	65	REG[02h] Configuration Readback Register	65
Clock Configuration Registers			
REG[20h] PLL M-Divider Register	66	REG[22h] PLL Setting Register 0	67
REG[24h] PLL Setting Register 1	67	REG[26h] PLL Setting Register 2	67
REG[28h] PLL Setting Register 3	67	REG[2Ah] PLL Setting Register 4	68
REG[2Ch] Clock Source Select Register	69	REG[2Eh] Power Save Register	70
TV Configuration Registers			
REG[40h] TV Display Configuration Register	71	REG[42h] TV Vertical Blanking Interval Data bits Register 0	72
REG[44h] TV Vertical Blanking Interval Data bits Register 1	72	REG[46h] TV Vertical Blanking Interval Data bits Register 2	72
REG[48h] TV Vertical Blanking Interval Data bits Register 3	72	REG[4Ah] VBI: Closed Caption / XDS Control / Status Register	76
REG[4Ch] TV DDS Fine Tuning Register 0	78	REG[4Eh] TV DDS Fine Tuning Register 1	78
REG[50h] TV Test Pattern Setting Register	80	REG[52h] TV Filter Setting Register	81
REG[54h] TV Filter Coefficient and User Clock Ratio Index Register	82	REG[56h] TV Filter Coefficient and User Clock Ratio Data Register	85
Input Data Control Registers			
REG[60h] Input Data Format Register	86	REG[62h] Special Effects Register	87
Input Window Size / Position Registers			
REG[64h] Host Input Window Height Register 0	94	REG[66h] Host Input Window Height Register 1	94
REG[68h] Host Input Window Width Register 0	94	REG[6Ah] Host Input Window Width Register 1	94
Display Output Control Registers			
REG[80h] Display Mode Register	95	REG[82h] Display Output Window X Start Position Register 0	96
REG[84h] Display Output Window X Start Position Register 1	96	REG[86h] Display Output Window Y Start Position Register 0	97
REG[88h] Display Output Window Y Start Position Register 1	97	REG[8Ah] Display Output Window Height Register 0	97
REG[8Ch] Display Output Window Height Register 1	97	REG[8Eh] Display Output Window Width Register 0	98
REG[90h] Display Output Window Width Register 1	98	REG[92h] Border Color Register 0	99
REG[94h] Border Color Register 1	99	REG[96h] Border Color Register 2	99
REG[98h] TV Transparency Color Register 0	100	REG[9Ah] TV Transparency Color Register 1	100
REG[9Ch] TV Transparency Color Register 2	100	REG[9Eh] DAC Reference Source Select Register	101

Table 11-2: S1D13746 Register Set (Continued)

Register	Pg	Register	Pg
Display Memory Access Registers			
REG[A0h] Display Memory Data Port Register 0	102		
3X3 Pixel Matrix Filter Registers			
REG[C0h] 3X3 Pixel Matrix Filter Control Register	103	REG[C2h] 3X3 Pixel Matrix Filter Coefficient Table Register 0	106
REG[C4h] 3X3 Pixel Matrix Filter Coefficient Table Register 1	107	REG[C6h] 3X3 Pixel Matrix Filter Coefficient Register 2	107
REG[C8h] 3X3 Pixel Matrix Filter Coefficient Table Register 3	107	REG[CAh] 3X3 Pixel Matrix Filter Coefficient Table Register 4	108
REG[CCh] 3X3 Pixel Matrix Filter Coefficient Table Register 5	108	REG[CEh] 3X3 Pixel Matrix Filter Coefficient Table Register 6	108
REG[D0h] 3X3 Pixel Matrix Filter Coefficient Register 7	109	REG[D2h] 3X3 Pixel Matrix Filter Coefficient Table Register 8	109
REG[D4h] 3X3 Pixel Matrix Filter Coefficient Table Register 9	109	REG[D6h] 3X3 Pixel Matrix Filter Coefficient Table Register 10	110
REG[D8h] 3X3 Pixel Matrix Filter Coefficient Table Register 11	110	REG[DAh] 3X3 Pixel Matrix Filter Coefficient Register 12	110
REG[DCh] 3X3 Pixel Matrix Filter Coefficient Table Register 13	111	REG[DEh] 3X3 Pixel Matrix Filter Coefficient Table Register 14	111
REG[E0h] 3X3 Pixel Matrix Filter Scale Value for Luminance Y Channel Register	111	REG[E2h] 3X3 Pixel Matrix Filter Scale Value for Chrominance U Channel Register	112
REG[E4h] 3X3 Pixel Matrix Filter Scale Value for Chrominance V Channel Register	112	REG[E6h] 3X3 Pixel Matrix Filter Offset Value for Luminance Y Channel Register	112
REG[E8h] 3X3 Pixel Matrix Filter Offset Value for Chrominance U Channel Register	113	REG[EAh] 3X3 Pixel Matrix Filter Offset Value for Chrominance V Channel Register	113
Miscellaneous Registers			
REG[ECh] Non-Display Period Control / Status Register	114	REG[EEh] Parallel RGB Interface Register	116
General Purpose IO Pins Registers			
REG[F0h] General Purpose IO Pins Configuration Register	117	REG[F2h] General Purpose IO Pins Status/Control Register	117
REG[F4h] GPIO Positive Edge Interrupt Trigger Register	117	REG[F6h] GPIO Negative Edge Interrupt Trigger Register	118
REG[F8h] GPIO Interrupt Status Register	118	REG[FAh] GPIO Pull Down Control Register	118

11.3 Register Descriptions

All reserved bits must be set to the default value. Writing a non-default value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect. Unless specified otherwise, all register bits are set to 0b during power-on reset.

Reserved registers must not be written. The Host must do a dummy read to reserved registers in Auto-Increment mode, or stop Auto-Increment after the last valid register before the reserved register and then re-start Auto-Increment from the next valid register.

11.3.1 Product Information Registers

REG[00h] Revision Code Register
Default = A9h — Read Only

Product Code bits 5-0						Revision Code bits 1-0	
7	6	5	4	3	2	1	0

bits 7-2 Product Code bits [5:0] (Read Only)
These bits indicate the product code. The product code for the S1D13746 is 101010b.

bits 1-0 Revision Code bits [1:0] (Read Only)
These bits indicate the revision code. The revision code is 01b.

REG[02h] Configuration Readback Register
Default = not applicable — Read Only

Macrovision Bond Option	n/a			CNF3 Status	CNF2 Status	CNF1 Status	CNF0 Status
7	6	5	4	3	2	1	0

bit 7 Macrovision Bond Option (Read Only)
When this bit = 0b, the Macrovision block is permanently disabled and can not be used, and REG[80h] bit 7 has no effect.
When this bit = 1b, the Macrovision block can be enabled (REG[80h] bit 7)

bits 3-0 CNF[3:0] Status (Read Only)
These status bits return the current status of the configuration pins CNF[3:0]. For a functional description of each configuration bit (CNF[3:0]), see Section 5.3, “Summary of Configuration Options” on page 29.

11.3.2 Clock Configuration Registers

REG[20h] PLL M-Divider Register
Default = 1Ah — Read/Write

PLL Lock (RO)	n/a	M-Divider bits 5-0					
7	6	5	4	3	2	1	0

bit 7 PLL Lock (Read Only)
This bit indicates the status of the PLL output. The maximum PLL lock time is 2.5ms. For further information, refer to Section 8.1.3, “PLL Clock” on page 36.
When this bit = 0b, the PLL output is not stable. In this state read/write access to the display buffer is prohibited.
When this bit = 1b, the PLL output is stable.

bits 5-0 M-Divider bits [5:0]
These bits determine the divide ratio between CLKI and the actual input clock to the PLL. The internal input clock to the PLL (PLLCLK) must be between 1 MHz and 2 MHz. Depending on CLKI, these bits will have to be set accordingly.

Table 11-3: PLL M-Divide Selection

REG[04h] Bits 5-0	M-Divide Ratio
0h	1:1
01h	2:1
02h	3:1
03h	4:1
• • •	• • •
1Ah (default	27:1
• • •	• • •
20h	33:1
21h to 3Fh	Reserved

REG[22h] PLL Setting Register 0
Default = F8h Read/Write

PLL Setting Register 0 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value F8h.

REG[24h] PLL Setting Register 1
Default = 80h Read/Write

PLL Setting Register 1 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value 80h.

REG[26h] PLL Setting Register 2
Default = 28h Read/Write

PLL Setting Register 2 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value 28h.

REG[28h] PLL Setting Register 3
Default = 00h Read/Write

PLL Setting Register 3 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value 00h.

REG[2Ah] PLL Setting Register 4							
Default = 35h							Read/Write
n/a	L-Counter bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 L-Counter bits [6:0]

These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (L-Counter + 1) x PLLCLK
= LL x (PLLCLK)

Where:

PLL Output is the desired PLL output frequency (in MHz).
L-Counter is the value of this register (in decimal).
PLLCLK is the internal input clock to the PLL (in MHz).

Table 11-4 Example PLL Clock Settings

CLKI Input Clock (MHz)	M-Divider REG[20h] bits 5-0	L-Counter REG[2Ah] bits 6-0	PLLCLK (MHz)	PLL Output (MHz)	TV DDS Clock Select (REG[2Ch] bit 2)	TV Timing Clock Select (REG[2Ch] bit 1)	TV Input Clock Setting (REG[4Eh] bits 5-4)	Program f_{sc}/f_{dds} and f_{timing}/f_{dds} REG[54h] ~ REG[56h]
27	26 (1Ah)	53 (35h)	1	54	0b	0b	00b	no
26	25 (19h)	53 (35h)	1	54	0b	1b	01b	no (see Note)
24	15 (0Fh)	35 (23h)	1.5	54	0b	1b	10b	yes
23	22 (16h)	53 (35h)	1	54	0b	1b	10b	yes
22	21 (15h)	53 (35h)	1	54	0b	1b	10b	yes
21	13 (0Dh)	35 (23h)	1.5	54	0b	1b	10b	yes
19.8	10 (0Ah)	29 (1Dh)	1.8	54	0b	1b	10b	yes
19.44	17 (11h)	49 (31h)	1.08	54	0b	1b	10b	yes
19.2	15 (0Fh)	44 (2Ch)	1.2	54	0b	1b	10b	yes
19	17 (11h)	53 (35h)	1	54	0b	1b	10b	yes
18	11 (0Bh)	35 (23h)	1.5	54	0b	1b	10b	yes

Note

For 26 MHz CLKI, f_{sc}/f_{dds} and f_{timing}/f_{dds} REG[54h] ~ REG[56h] must be programmed for NTSC M/J.

REG[2Ch] Clock Source Select Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a					TV DDS Clock Source Select	TV Timing Clock Source Select	SYSCLK Source Select

bit 2 TV DDS Clock Source Select

This bit selects the TV DDS clock source. For details on the clock structure, see Section 9, “Clocks” on page 59.

When this bit = 0b (default), the TV DDS clock source is the external Clock input (CLKI or OSCx).

When this bit = 1b, the TV DDS clock source is the internal PLL ‰ 2.

bit 1 TV Timing Clock Source Select

This bit selects the TV Timing clock source. If CLKI is 27MHz, this bit can be set to 0b. If CLKI is not 27MHz, the PLL must be programmed to 54MHz (see Table 11-4 “Example PLL Clock Settings,” on page 68) and this bit should be set to 1b. For details on the clock structure, see Section 9, “Clocks” on page 59.

When this bit = 0b, the TV Timing clock source is the external Clock input (CLKI or OSCx).

When this bit = 1b, the TV Timing clock source is the internal PLL ‰ 2.

bit 0 SYSCLK Source Select

This bit selects the system clock (SYSCLK) source for the S1D13746. For more information on the PLL and clock structure, see Section 9, “Clocks” on page 59.

When this bit = 0b, the SYSCLK source is the external Clock input (CLKI or OSCx).

When this bit = 1b, the SYSCLK source is the internal PLL.

If the PLL is to be selected as the SYSCLK source, the PLL must be configured before setting this bit. To configure the PLL, sleep mode needs to be enabled (REG[2Eh] bit 1 = 1b). Once in sleep mode, REG[20h] and REG[2Ah] can be changed to set the desired PLL frequency. Once REG[20h] and REG[2Ah] have been set, REG[2Ch] bit 0 can be set to 1b to select the PLL as system clock source.

Note

There may be up to a 2.5ms delay before the PLL output becomes stable. The display memory must not be accessed before PLL output is stable. The PLL Lock bit (REG[20h] bit 7), can be used to determine if the PLL output is stable.

REG[2Eh] Power Save Register
Default = 00h Read/Write

PWRSVE Input Pin Function	n/a					Sleep Mode Enable	Standby Mode Enable
7	6	5	4	3	2	1	0

bit 7 PWRSVE Input Pin Function

This bit determines the functionality of the PWRSVE input pin.
When this bit = 0b, the PWRSVE pin is ORed with the Sleep Mode Enable bit (REG[2Eh] bit 1) and setting either to 1b will enable Sleep Mode.
When this bit = 1b, the PWRSVE pin is ORed with the Standby Mode Enable bit (REG[2Eh] bit 0) and setting either to 1b will enable Standby Mode.

bit 1 Sleep Mode Enable

This bit controls the Sleep power save mode. Sleep mode can also be controlled by the PWRSVE pin when REG[2Eh] bit 7 = 0b.
When this bit = 0b, Sleep Mode is disabled (normal operation).
When this bit = 1b, Sleep Mode is enabled.

When Sleep Mode is enabled, all internal blocks, including the PLL, are disabled.
When Sleep Mode is disabled, the PLL requires approximately 2.5ms lock time before any memory access should be attempted. The PLL Lock bit, REG[20h] bit 7, can be read to verify when the PLL becomes stable.

Note

IREF/VREF and TV OUT must be disabled before entering Sleep Mode. Set REG[9Eh] bits 1-0 = 00b and REG[80h] bit 2 = 0b.

bit 0 Standby Mode Enable

This bit controls the Standby power save mode. Standby mode can also be controlled by the PWRSVE pin when REG[2Eh] bit 7 = 1b.
When this bit = 0b, Standby Mode is disabled (normal operation).
When this bit = 1b, Standby Mode is enabled.

When Standby Mode is enabled, all internal blocks are disabled except for the PLL.
When Standby Mode is disabled, the S1D13746 can be accessed immediately.

11.3.3 TV Configuration Registers

REG[40h] TV Display Configuration Register							
Default = 00h							Read/Write
Reserved	VBI Selection bits 1-0		Output Signal Format	TV Standard Select bits 2-0			n/a
4	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0b.

bits 6-5 VBI Selection bits [1:0]
These bits control the Wide-Screen signalling standard.

Table 11-5: Wide-Screen Signalling Standard

REG[40h] bits 6-5	Standard
00b (default)	No VBI Data (default)
01b	Enable WSS according to ITU-R BT.1119-2 standard
10b	Enable WSS + CGMS + APS according to CEI 61880
11b	Enable the Closed Caption and XDS according to CEA-608-B

bit 4 Output Signal Format
This bit determines the format of the TV output signal.
When this bit = 0b, the output signal format is composite video.
When this bit = 1b, the output signal format is S-Video.

bits 3-1 TV Standard Select bits [2:0]
These bits select the TV standard and sub-standard as follows.

Table 11-6: TV Standard Selection

REG[40h] bits 3-1	TV Standard	Sub-Standard
000b (default)	625 Line System	PAL B, D, G, H, I
001b	525 Line System	PAL M
010b	625 Line System	PAL N
011b	625 Line System	PAL Nc
100b	525 Line System	NTSC M
101b	525 Line System	NTSC J
110b - 111b	Reserved	

REG[42h] TV Vertical Blanking Interval Data bits Register 0
Default = 00h Read/Write

VBI Data bits 7-0							
7	6	5	4	3	2	1	0

REG[44h] TV Vertical Blanking Interval Data bits Register 1
Default = 00h Read/Write

VBI Data bits 15-8							
7	6	5	4	3	2	1	0

REG[46h] TV Vertical Blanking Interval Data bits Register 2
Default = 00h Read/Write

VBI Data bits 23-16							
7	6	5	4	3	2	1	0

REG[48h] TV Vertical Blanking Interval Data bits Register 3
Default = 00h Read/Write

VBI Data bits 31-23							
7	6	5	4	3	2	1	0

REG[48h] bits 7-0
REG[46h] bits 7-0
REG[44h] bits 7-0
REG[42h] bits 7-0 VBI Data bits [31:0]
These bits configure the data required for wide-screen signalling. The data set differs based on the TV standard (see REG[40h] bits 6-5).

Table 11-7: VBI Data Bit Descriptions (ITU-R BT.1119-2 / ETSI EN 300 294 625 and 525 Line systems)

VBI Data bit	PAL			NTSC		
	Bit No	Name	Desc.	Bit No.	Name	Desc.
0	0	Aspect Ratio	1000b: Full format 4:3 0001b: Box 14:9 center 1010b: Box 14:9 top 1011b: Box 16:9 center 0100b: Box 16:9 top 1101b: Box > 16:9 center 1110b: Full format 14:9 or center shoot and protect 14:9 0111b: Full format 16:9 anamorphic	1	Reference	Should be set to 1b
1	1			2	Reference	Should be set to 0b
2	2			3	Aspect Ratio	0b: 4:3 full format 1b: 16:9 letter box
3	3			4	Parity	Even parity for bit no. 3 ~ 5 (B3 ~ B5)
4	4	Film bit	0b: Camera mode 1b: Film mode	5	Reserved	Should be set to 0b
5	5	Color Coding bit	0b: conventional coding 1b: Motion Adaptive Color Plus	6	Field Type Active	0b: Field type not active, output = 0. 1b: Field type active, output = 0 for first field, output = 1 for next field.
6	6	Helper bit	0b: No helper 1b: Modulated helper	7	Frame Type Active	0b: Frame type not active, output = 0. 1b: Frame type active, output = 0 for reference frame, output = 1 for other frame.
7	7	Reserved	Should be set to 0b	8	Vertical Temporal Helper	0b: No. 1b: Yes.
8	8	Subtitles Within Teletext bit	0b: No subtitles within teletext 1b: Subtitles within teletext	9	Vertical High Resolution Helper	0b: No. 1b: Yes.
9	9	Subtitling Mode	00b: No open subtitles 01b: Subtitles in active image area 10b: Subtitles out of active image area 11b: Reserved	10	Horizontal Helper	0b: No. 1b: Yes.
10	10			11	Horizontal Helper Pre-Combing	0b: No. 1b: Yes.
11	11	Reserved	0b: see Note	12	Assigned for use in TV broadcasting stations	
12	12		0b: see Note	13		
13	13		0b: see Note	14		Should be set to 0b
14				15	Reserved	Should be set to 0b
15				16		
16				17		
17				18	Error Correction Codes	CRC codes for bit no. 3 ~ 17 (B3 ~ B17): G(x) = X^6 + X + 1
18				19		
19				20		
20				21		
21				22		
22				23		
23				24	Reference	Should be set to 0b

Note

For ITU-R BT.1119-2 bits 13 ~ 11 are reserved and should be written 000b
For ETSI EN 300 294 these bits have the following functions:

bit 11	Surround Sound	0b = no surround sound information 1b = surround sound mode
bit 12	Copy Right	0b = no copy right asserted or status unknown 1b = copy right asserted
bit 13	Copying	0b = copying not restricted 1b = copying restricted

Table 11-8: VBI Data Bit Descriptions (CEI 61880, 525 Line systems)

VBI Data bit	For NTSC System Only		
	Bit No	**Name**	**Description**
0	1	Reference Bit	set to 1b
1	2	Reference Bit	set to 0b
2	3	Aspect Ratio	Bits 4-3 00b: Normal 4:3 01b: Normal 16:9 10b: Letter Box 4:3 11b: Reserved:
3	4		
4	5	Copy Control Information	Bits 8-5 0000b: The bits 14-7 (CGMS-A, APS trigger, ASB bits) are transferred. 1111b: The bits 14-7 are not transferred (bits 14-7 are set to 0b).
5	6		
6	7		
7	8		
8	9	CGMS-A bits	Bits 10-9 00b: Copying is permitted without restriction 01b: One generation of copies may be made 10b: Condition not to be used 11b: No copying is permitted
9	10		
10	11	APS trigger bits	Bits 12-11 00b: PSP off 01b: PSP on, 2-line split burst on 10b: PSP on, split burst off 11b: PSP on, 4-line split burst on
11	12		
12	13	Analogue source bit	1b: Analog pre-recorded packaged medium. 0b: Not Analog pre-recorded packaged medium.
13	14		Shall be set to 0b
14	15		
15	16		
16	17	CRCC bits	$G(x) = X^6 + X + 1$
17	18		
18	19		
19	20		
20	21		
21	22		
22			Must be set to 0b
23			Must be set to 0b
24			Must be set to 0b
25			Must be set to 0b
26			Must be set to 0b
27			Must be set to 0b
28 - 31			Must be set to 0b

Table 11-9: VBI Data Bit Descriptions (CEA-608-B)

VBI Data bit	REG[4Ah] bit 1 = 0b (in auto WSS+CMGS+APS mode) See Table 11-10: when REG[4Ah] bit 1 = 1b		
	Bit No.	**Name**	**Desc.**
0	1	S0.	Aspect Ratio Information: Start Position The S0 to S5 bits define the Starting line number for active picture information. The starting line number is computed by adding 22 (for 525-line System) to the decimal number represented by bits S0 to S5.
1	2	S1	
2	3	S2	
3	4	S3	
4	5	S4	
5	6	S5	
6	7	E0	Aspect Ratio Information: End Position The E0 to E5 bits define the Ending line number for active picture information. The ending line number is calculated by subtracting the decimal number represented by bits E0 to E5 from 262 (for 525-line System).
7	8	E1	
8	9	E2	
9	10	E3	
10	11	E4	
11	12	E5	
12	13	Q0	This bit indicates if the video is squeezed (Q0=1b) or normal (Q0=0b). Squeezed video results from compressing an original 16 X 9 image into 4 X 3 format without cropping off the side panels.
13	14	ASB	the Analog Source Bit.
14	15	APS, bit0	APS Bits 1-0 00b: No APS 01b: PSP On; Split Burst Off 10b: PSP On; 2 line Split Burst On 11b: PSP On; 4 line Split Burst On
15	16	APS, bit1	
16	17	CGMS-A, bit0	CGMS-A Bits 1-0 00b: Copying is permitted without restriction 01b: Condition not to be used 10b: One generation of copies may be made 11b: No copying is permitted
17	18	CGMS-A, bit1	
18	19	Reserved	The second byte of the “Copy Generation Management System” is reserved for future use. All reserved bits shall be zero.
19	20		
20	21		
21	22		
22	23		
23	24		
24	25		Bits 27-25 - Auto XDS Packet Refresh Rate bits 2-0 This 3-bit register defines the refresh rate for the two XDS packets, “Aspect Ratio Information” and “Copy Generation Management System”. The two XDS packets are sent out every 8*(the value of this register + 1) /25 seconds for PAL, 8*(the value of this register + 1) /30 seconds for NTSC.
25	26		
26	27		
27 - 31	28 - 32	Reserved	Must be set to 0b

Table 11-10: VBI Data Bit Descriptions for XDS (CEA 608-B)

VBI Data bit	And REG[4A] bit 1 = 1b (in auto WSS+CGMS+APS disable mode) See Table 11-9: when REG[4A] bit 1 = 0b		
	Bit Number	**Name**	**Description**
0-6	1-7	XDS Byte 1, D[0:6]	The first ASCII Character sent out on the Line21/22 field 1
8-14	9-15	XDS Byte 2, D[0:6]	The second ASCII Character sent out on the Line21/22 field 1
16-22	17-23	XDS Byte 3, D[0:6]	The first ASCII Character sent out on the Line284/384 field 2
24-30	25-31	XDS Byte 4, D[0:6]	The second ASCII Character sent out on the Line284/384 field 2

REG[4Ah] VBI: Closed Caption / XDS Control / Status Register
Default = 10h — Read/Write

7	6	5	4	3	2	1	0
Reserved			Frame VSYNC Period (RO)	Field 2 Data Valid	Field 1Data Valid	CEA 608-B Line 21 Data Service Auto Mode Disable	VBI Enable

bits 7-5 Reserved
The default value for these bits is 000b.

bit 4 Frame VSYNC Period (Read Only)
When this bit = 0b, it indicates the time interval when TV Frame VSYNC is not active
When this bit = 1b, it indicates the time interval when TV Frame VSYNC is active

During the active TV Frame VSYNC period, the host can update the VBI Data Registers (REG[46h] ~ REG[4Ch]) and bits 3 ~ 0 of this register. When not in an active TV Frame VSYNC period, the host should not update the VBI Data Registers and bits 3 ~ 0 of this register.

The active TV Frame VSYNC time interval depends on the TV standard set with REG[40h] bits 3-1.

For for PAL B/D/G/H/I/Nc between lines 624 and 16
For for PAL N between lines 623 and 15
For for NTSC M/J between lines 1 to 18
For for PAL M between lines 523 and 15

bit 3 Field 2 Data Valid
When this bit = 0b, VBI Data bits 30-16 are invalid or have already been sent out on the previous Field 2.
Write a 1b to this bit when REG[4Eh] bit 4 = 1b to send VBI Data bits 30-16 out at the next field 2.

Note

1. This bit is only valid when bit 1 = 1b and REG[44h] bits 6-5 = 11b.
2. Check REG[4Eh] bit 4 = 1b before updating this bit.

bit 2 Field 1 Data Valid

When this bit = 0b, VBI Data bits 14-0 are invalid or have already been sent out on the previous Field 1.

Write a 1b to this bit when REG[4Eh] bit 4 = 1b to send VBI Data bits 14-0 out at the next field 1.

Note

1. This bit is only valid when bit 1 = 1b and REG[44h] bits 6-5 = 11b.
2. Check REG[4Eh] bit 4 = 1b before updating this bit.

bit 1 CEA 608-B Line 21 Data Service Auto Mode Disable

When this bit = 0b, the VBI Data + CGMS + APS is combined with the XDS sequence and sent out automatically on field 2 packets (field 1 packets are sent as zero data packets). Refer to Table 11-9: “VBI Data Bit Descriptions (CEA-608-B),” on page 75 for more information on the field 2 packet data transfer information.

When this bit = 1b, the CEA 608-B Line 21 Data Service Auto Mode is disabled and REG[4E] bits [4:2] are used in conjunction with REG[46h ~ 4Ch] to send the XDS sequence manually on field 1 or 2 packets. Refer to Table 11-10: “VBI Data Bit Descriptions for XDS (CEA 608-B),” on page 76 more information on the field 1 and 2 packet data transfer information.

Note

This bit is only valid when REG[40h] bits 6-5 = 11b.

bit 0 VBI Enable

When this bit = 0b, the VBI is disabled.

When this bit = 1b, the VBI is enabled.

REG[4Ch] TV DDS Fine Tuning Register 0
Default = 00h Read/Write

Reserved							
7	6	5	4	3	2	1	0

REG[4Eh] TV DDS Fine Tuning Register 1
Default = 00h Read/Write

Reserved		TV Clocks Setting bits 1-0		n/a	Reserved		
7	6	5	4	3	2	1	0

REG[4Eh] bits 2-0
REG[4Ch] bits 7-0 Reserved
The default value for these bits is 000_0000_0000b.

REG[4Eh] bits 7-6 Reserved
The default value for these bits is 00b.

REG[4Eh] bits 5-4 TV Clocks Setting bits [1:0]
These bits are used in conjunction with CLKI frequency, REG[2Ch] bits 2-1, and REG[54h] ~ REG[56h] to set the clocks for the TV block.

Table 11-11: TV Input Clock Setting

REG[4Eh] bits 5-4	f_{timing} (frequency of the Clock used for Timing)	f_{dds} (frequency of the Clock used for internal DDS and DAC)
00b	27MHz	27MHz
01b	27MHz	26MHz
10b	27MHz	18 ~ 27MHz (Notes 1 and 2)
11b	Reserved	

Table 11-12: TV Clock Settings

CLKI Frequency (MHz)	TV Input Clock Setting (REG[4Eh] bits 5-4)	TV DDS Clock Select (REG[2Ch] bit 2) (see Note)	TV Timing Clock Select (REG[2Ch] bit 1)	Need to Program f_{sc}/f_{dds} and f_{timing}/f_{dds} Ratios?
27	00b	0b (CLKI)	0b (CLKI)	No
26	01b	0b (CLKI)	1b (PLL ‰ 2 = 27MHz)	No (Note 1)
18 ƒ CLKI ƒ 27	10b	0b (CLKI)	1b (PLL ‰ 2 = 27MHz)	Yes (Note 2)
1 ƒ CLKI ƒ 18	00b	1b (PLL ‰ 2 = 27MHz) (Note 3)	1b (PLL ‰ 2 = 27MHz)	No

Note

1. If REG[4Eh] bits 5-4 = 10b, (CLKI is not 27MHz or 26MHz), the f_{sc}/f_{dds} registers (REG[54h] Index 20~27 and REG[56h]) must be programmed with the correct values for NTSCM or NTSCJ.
2. If REG[4Eh] bits 5-4 = 10b and CLKI is less than 26MHz, the SCH Phase error cannot meet the consumer grade specification of within 20 degrees.
3. REG[2Ch] bit 2 allows the DDS clock to be selected from the PLL. However, due to PLL jitter there is no guarantee that all timings will be met as per ITU-BT470 or SMPTE170M.

REG[50h] TV Test Pattern Setting Register
Default = 00h Read/Write

Luminance Delay Setting 3-0				Test Pattern Select bits 3-0			
7	6	5	4	3	2	1	0

bits 7-4 Luminance Delay Setting bits [3:0]
These bits determine the delay between the Luminance and Chrominance data for S-Video output (REG[40h] bit 4 = 1b).
Luminance delay = {(REG[50h] bits 7-4) x 37ns}
where REG[50h] bits 7-4 is a value between 0000b to 1100b
(0ns -----> 12 x 37ns range in 37ns increments)

bits 3-0 Test Pattern Select bits [3:0]
These bits select the built-in TV test patterns from the test pattern generator.

Table 11-13: Test Pattern Definitions

REG[50h] bits 3-0	Test Pattern Description	Notes
0000b	Test Pattern Generator Disabled	Normal operation
0001b	75% Color Bar with 75% white	Start from 10.3us, every 6.7us
0010b	100% Color Bar	
0011b	75% Color Bar with 100% white	
0100b	Reserved	
0101b	Constant Y (77IRE, YCbCr: 180/128/128)	all line active as hde
0110b	Constant Y + Red (YCbCr: 65/100/212)	
0111b	10-step staircase without chrominance	4us every step start from 13.5us
1000b	Ramp Y without chrominance	from 20.2us to 53.0us
1001b	10-step staircase with chrominance 1 (CbCr: 89/156)	for PAL
1010b	10-step staircase with chrominance 2 (CbCr: 73/128)	for NTSC
1011b	Ramp A with chrominance 1 (*UV: -20/20*)	for PAL
1100b	Ramp A with chrominance 2 (*UV: -28/0*)	for NTSC
1101b	100IRE Ramp with color A: n/-21/21, n: 0 -140	for NTSC
1110b	100IRE Ramp with color B: n/-28/0, n: 0 -140	for PAL
1111b	80IRE Ramp with color A: n/-21/21, n: 0 -448	for NTSC

Table 11-14: Test Pattern Usage for Each Video Parameter

Item/Parameters	Requirement	Test Signals
Differential Phase	< 4^o	A modulated staircase (5 or 10) or a modulated ramp, $0^o \pm 1^o$ to the burst
Differential Gain	< 4%	10--step modulated staircase
Hue Accuracy	< 3^o	color bar
Saturation Accuracy	< 3%	color bar
SNR	> 48 dB	
SCH phase	40^o	any signals with color burst
Subcarrier Tolerance	< 2/1 Hz (NTSC/PAL)	

REG[52h] TV Filter Setting Register
Default = 00h Read/Write

Dot-Crawl Elimination Disable	n/a		Reserved		Programmable Filter Select	Chrominance Filter Enable	Luminance Filter Enable
7	6	5	4	3	2	1	0

bit 7 Dot-Crawl Elimination Disable

This bit selects whether the NTSC Dot-Crawl Elimination circuit is enabled or disabled. This bit has an effect only if NTSC M or NTSC J is selected (REG[40h] bits 3-1 = 100b or 101b) and composite video is selected as the output signal format (REG[40h] bit 4 = 0b). For PAL standard or S-video output signal the NTSC Dot-Crawl Elimination circuit is disabled.

When this bit = 0b, the NTSC Dot-Crawl Elimination Circuit is enabled.

Note

This bit should be programmed to 0b only if the following conditions are satisfied:

a. NTSC M or NTSC J is used
b. Composite video output is used
c. The display is a CRT display

When this bit = 1b, the NTSC Dot-Crawl Elimination Circuit is disabled.

bits 4-3 Reserved

The default value for these bits is 00b.

bit 2 Programmable Filter Select

This bit selects whether the filter parameters for the chrominance/luminance filters are pre-programmed or programmable using the registers REG[54h] and REG[56h].

When this bit = 0b, the filter parameters are pre-programmed according to the TV standard.

When this bit = 1b, the filters parameters are programmable through registers.

See Section 22, “TV Filter Operation” on page 176 for further information.

bit 1 Chrominance Filter Enable

This bit controls the chrominance filter function.

When this bit = 0b, the chrominance filter is disabled.

When this bit = 1b, the chrominance filter is enabled.

bit 0 Luminance Filter Enable

This bit controls the luminance filter function.

When this bit = 0b, the luminance filter is disabled.

When this bit = b1, the luminance filter is enabled.

REG[54h] TV Filter Coefficient and User Clock Ratio Index Register
Default = 00h Read/Write

Reserved	n/a	TV Filter Coefficient and User Clock Ratio Index bits 5-0					
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0b.

bits 5-0 TV Filter Coefficient and User Clock Ratio Index bits [5:0]
The Luminance Filter is a 15-tap FIR filter which can be configured as a notch or low-pass filter. The Chrominance Filter is a 15-tap low-pass FIR Filter.

There are 8 Chrominance coefficients (16 bytes) each having a sign bit associated with it. There are 8 Luminance coefficients (16 bytes) each having a sign bit associated with it. There is one register (4 bytes) which defines the ratio f_{timing}/f_{dds}, and one register (4 bytes) which defines the ratio f_{sc}/f_{dds}. This Index register provides access to the 40 bytes of data accessed through REG[56h].

Index 00h ~ 1Fh
The first 16 bytes are the Luminance coefficients and the next 16 bytes are the Chrominance coefficients (every coefficient has 2 bytes, first byte = coefficient, second byte, bit 0 = sign bit).

Index 20h ~ 23h
These 4 bytes set the ratio between TV timing clock (f_{timing}) and the DDS clock (f_{dds}). This clock ratio must be programmed when TV timing clock is not 27 MHz or 26 MHz, REG[4Eh] bits 5-4 is 10b. The 30-bit value is equal to $f_{timing}/f_{dds} \times 2^{29}$. The default value is 0.

Index 24h ~ 27h
These last 4 bytes set the ratio between the subcarrier clock (f_{sc}) and the DDS clock (f_{dds}). This clock ratio must be programmed based on the TV standard (REG[40h] bits 3-1) when DDS clock is not 27 MHz or 26 MHz (REG[4Eh] bits 5-4 is 10b) or when DDS clock is 26 MHz and NTSCM or NTSCJ is selected (REG[4Eh] bits 5-4 = 01b and REG[40h] bits 3-1 = 100b or 101b). The 30-bit value is equal to $f_{sc}/f_{dds} \times 2^{32}$.

Note
The f_{sc}/f_{dds} ratio is based on the TV standard. Therefore, it must be reprogrammed if the TV standard is changed in REG[40h] bits 3-1.

Example

If CLKI is 18 MHz and the TV standard is NTSCM:

Sub Carrier f_{sc} is 3.5795454MHz

DDS clock f_{dds} is 18MHz

TV timing clock f_{timing} is 27MHz,

REG[2Ch] bits 2-1 should be set 01b

REG[4Eh] bits 5-4 should be set 10b.

Clock Ratio $f_{timing}/f_{dds} = 27/18 \times 2^{29} = 805,306,368 = 3000\_0000h$.

The 4 bytes indexed from 20h to 23h in REG[54h] should be programmed as 00h, 00h, 00h, and 30h in REG[56h].

Clock Ratio $f_{sc}/f_{dds} = 3.5795454/18 \times 2^{32} = 854,112,802 = 32E8\_BA21h$.

The last 4 bytes indexed from 24h to 27h in REG[54h] should be programmed as 21h, BAh, E8h, and 32h in REG[56h].

Note

The Luminance and Chrominance Filters have the following default values.

Table 11-15: Default Luminance Filter Values

REG[52h] bit 2	REG[40h] bit 4	TV Standard	Coefficient 0	Coefficient 1	Coefficient 2	Coefficient 3	Coefficient 4	Coefficient 5	Coefficient 6	Coefficient 7	Note
0b	1b	-	1FDh	005h	1FCh	1FDh	012h	1DAh	036h	0C3h	low-pass
0b	0b	NTSC, M/Nc PAL	1FDh	006h	00Ah	1E6h	1F1h	036h	008h	0BDh	Notch Filter @ 3.58MHz
0b	0b	(B,D,G, H,I,N) PAL	003h	1F6h	00Ah	00Eh	1D5h	01Ch	01Eh	0BFh	Notch Filter @ 4.43MHz
1b	-	-	Register values used								User Configuration

Table 11-16: Default Chrominance Filter Values

REG[52h] bit 2	Coefficient 0	Coefficient 1	Coefficient 2	Coefficient 3	Coefficient 4	Coefficient 5	Coefficient 6	Coefficient 7	Note
0b	001h	001h	1FBh	1F5h	1FDh	01Dh	047h	05Bh	low-pass [1.5db attenuation @ 1.3MHz, > 20db at 3.6MHz]
1b	Register values used								User Configuration

Table 11-17: Chrominance / Luminance Filter Coefficient Index

Index	Description	Index	Description
00h	luminance filter coefficient 0 register 0 (bits 7-0)	14h	chrominance filter coefficient 2 register 0 (bits 7-0)
01h	luminance filter coefficient 0 register 1 (sign bit)	15h	chrominance filter coefficient 2 register 1 (sign bit)
02h	luminance filter coefficient 1 register 0 (bits 7-0)	16h	chrominance filter coefficient 3 register 0 (bits 7-0)
03h	luminance filter coefficient 1 register 1 (sign bit)	17h	chrominance filter coefficient 3 register 1 (sign bit)
04h	luminance filter coefficient 2 register 0 (bits 7-0)	18h	chrominance filter coefficient 4 register 0 (bits 7-0)
05h	luminance filter coefficient 2 register 1 (sign bit)	19h	chrominance filter coefficient 4 register 1 (sign bit)
06h	luminance filter coefficient 3 register 0 (bits 7-0)	1Ah	chrominance filter coefficient 5 register 0 (bits 7-0)
07h	luminance filter coefficient 3 register 1 (sign bit)	1Bh	chrominance filter coefficient 5 register 1 (sign bit)
08h	luminance filter coefficient 4 register 0 (bits 7-0)	1Ch	chrominance filter coefficient 6 register 0 (bits 7-0)
09h	luminance filter coefficient 4 register 1 (sign bit)	1Dh	chrominance filter coefficient 6 register 1 (sign bit)
0Ah	luminance filter coefficient 5 register 0 (bits 7-0)	1Eh	chrominance filter coefficient 7 register 0 (bits 7-0)
0Bh	luminance filter coefficient 5 register 1 (sign bit)	1Fh	chrominance filter coefficient 7 register 1 (sign bit)
0Ch	luminance filter coefficient 6 register 0 (bits 7-0)	20h	f_{timing}/f_{dds} ratio [7:0]
0Dh	luminance filter coefficient 6 register 1 (sign bit)	21h	f_{timing}/f_{dds} ratio [15:8]
0Eh	luminance filter coefficient 7 register 0 (bits 7-0)	22h	f_{timing}/f_{dds} ratio [23:16]
0Fh	luminance filter coefficient 7 register 1 (sign bit)	23h	f_{timing}/f_{dds} ratio [29:24]
10h	chrominance filter coefficient 0 register 0 (bits 7-0)	24h	f_{sc}/f_{dds} ratio [7:0]
11h	chrominance filter coefficient 0 register 1 (sign bit)	25h	f_{sc}/f_{dds} ratio [15:8]
12h	chrominance filter coefficient 1 register 0 (bits 7-0)	26h	f_{sc}/f_{dds} ratio [23:16]
13h	chrominance filter coefficient 1 register 1 (sign bit)	27h	f_{sc}/f_{dds} ratio [29:24]

Table 11-18: Common f_{timing}/f_{dds} and f_{sc}/f_{dds} Ratios

f_{dds} (CLKI Frequency) (MHz)	Ratio (f_{timing}/f_{dds}) x 2^{29}	f_{timing}/f_{dds} Ratio Value (hex)	TV Standard	f_{sc} (MHz)	Ratio (f_{sc}/f_{dds}) x 2^{32}	f_{sc}/f_{dds} Ratio Value (hex)
18	805306368	30000000	NTSC	3.5795454	854112802	32E8BA21
18			PAL-M	3.57561149	853174134	32DA6776
18			PAL-Nc	3.58205625	854711914	32F1DE69
18			PAL - Others	4.43361875	1057902641	3F0E5030
19.2	754974720	2D000000	NTSC	3.5795454	800730751	2FBA2E7F
19.2			PAL-M	3.57561149	799850751	2FACC0FE
19.2			PAL-Nc	3.58205625	801292419	2FC2C083
19.2			PAL - Others	4.43361875	991783726	3B1D6B2D
26	557519793	213B13B1	NTSC	3.5795454	591308863	233EA83F
26			PAL-M	3.57561149	590659016	2334BDC8
26			PAL-Nc	3.58205625	591723633	2344FC71
26			PAL - Others	4.43361875	732394136	2BA77298

REG[56h] TV Filter Coefficient and User Clock Ratio Data Register
Default = 00h Read/Write

TV Filter Coefficient and User Clock Ratio Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 TV Filter Coefficient and User Clock Ratio Data bits [7:0]
This register specifies the data to be R/W based on the above indexed address (REG[54h] bits 4-0). Continuous write access to this register will auto increment the address above (REG[54h] bits 5-0).

REG[58h] through REG[5Ah] are Reserved

These registers are reserved and must not be written.

11.3.4 Input Data Control Registers

REG[60h] Input Data Format Register
Default = 30h Read/Write

n/a		YUV Input Data Type Select bits 1-0		Input Data Format Select bits 3-0			
7	6	5	4	3	2	1	0

bits 5-4 YUV Input Data Type Select bits [1:0]
These bits define the YUV data type of input data to the S1D13746. The YUV input data is always converted to YCbCr before being written to the memory. The default type is YCbCr.

Table 11-19: YUV Data Type Selection

REG[60h] bits 5-4	Data Type	YRC Input Data Range
00b	YUV	0 ƒ Y ƒ 255 -128 ƒ U ƒ 127 -128 ƒ V ƒ 127
01b	YCbCr	16 ƒ Y ƒ 235 -113 ƒ U ƒ 112 -113 ƒ V ƒ 112
10b	YUV Offset	0 ƒ Y ƒ 255 0 ƒ U ƒ 255 0 ƒ V ƒ 255
11b (default)	YCbCr Offset	16 ƒ Y ƒ 235 16 ƒ U ƒ 240 16 ƒ V ƒ 240

bits 3-0 Input Data Format Select bits [3:0]

These bits select the input data format. For details on individual data formats, see Section 12, “Intel 80, 8-Bit Interface Color Formats” on page 119, Section 13, “Intel 80, 16-bit Interface Color Formats” on page 123, and Section 14, “YUV Timing” on page 129.

Table 11-20: Input Data Format Selection

REG[60h] bits 3-0	Input Data Format
0000b	RGB 3:3:2
0001b	RGB 5:6:5
0010b	RGB 6:6:6 Mode 1
0011b	RGB 8:8:8 Mode 1
0100b	Reserved
0101b	Reserved
0110b	RGB 6:6:6 Mode 2 (note 3)
0111b	RGB 8:8:8 Mode 2 (note 3)
1000b	YUV 4:2:2
1001b	YUV 4:2:0
1010b - 1111b	Reserved

Note

1. All input data is converted and stored as YUV 4:2:0.
2. When using the Parallel RGB interface to input image data (CNF[1:0] = 00b or 10b), REG[60h] bit 3 must be set to 0b.
3. RGB 6:6:6 Mode 2 and RGB 8:8:8 Mode 2 are only supported for the 16-bit Intel 80 interface (CNF[1:0] = 11b).

REG[62h] Special Effects Register

Default = 00h Read/Write

7	6	5	4	3	2	1	0
Window Data Type	Double Buffer Enable	Background Window	Square Pixel Correction Enable	Transparency Select bits 1-0		Window Rotation bits 1-0	

bit 7 Window Data Type

This bit determines the data type for the window. For use case examples and double-buffer information, see Section 20, “Typical Use Case Descriptions” on page 159 and Section 21, “Double Buffer Description” on page 173.

When this bit = 0b, the data being written from the Host is considered “static” and is not double-buffered.

When this bit = 1b, the data being written from the Host is considered “streaming” and requires double-buffering (REG[62h] bit 6 = 1b).

bit 6 Double-Buffer Enable

This bit is used to enable the Double-Buffer. For use case examples and double-buffer information, see Section 20, “Typical Use Case Descriptions” on page 159 and Section 21, “Double Buffer Description” on page 173.
When this bit = 0b, the Double-Buffer is disabled for the window being written / activated.
When this bit = 1b, the Double-Buffer is enabled for the window being written / activated to prevent image tearing with streaming data.

When a Parallel RGB interface is selected (see CNF[1:0]), the following restrictions must be met or the Double-Buffer should not be used.

- The input frame rate must be smaller than half of the output (display frame rate).
- The input data burst must be shorter than the output frame period.

bit 5 Background Window

This bit is used to change the input image type from background to destructive overlay. For use case examples and double-buffer information, see Section 20, “Typical Use Case Descriptions” on page 159 and Section 21, “Double Buffer Description” on page 173.
When this bit = 0b, the window being written is considered a destructive overlay
When this bit = 1b, the window being written is considered the background image

Note
For the Parallel RGB Host Interface (CNF[1:0] = 00 or 10), this bit must be set to 1b.

bit 4 Square Pixel Correction Enable

When images are displayed on a calibrated TV, the length of a given number of pixels horizontally is not the same as the length of the same number of pixels vertically. For example, with a calibrated NTSC TV, a box which is 8x8 pixels will not look like a square but rather the width will look shorter than the height. When square pixel is enabled, the width of the output image will be scaled appropriately by the S1D13746 to make an NxN image look like a square. The square pixel scaling logic takes into account which TV standard (PAL or NTSC) is selected and scales accordingly. For NTSC, the image will be widened. For PAL, the image will be narrowed.

When this bit = 0b, Square Pixel correction is disabled. (default)
When this bit = 1b, Square Pixel correction is enabled.

Table 11-21: Square Pixel Correction

REG[62h] bit 4	TV Standard	Scaling Ratio	Maximum Output Width Setting
0	—	256/256 (1.000)	720
1b	NTSC	282/256 (1.101)	654 (654 x 282 ‰ 256 = 720)
1b	PAL	234/256 (0.914)	788 (788 x 234 ‰ 256 = 720)

Note
Square Pixel Correction is not supported for PALM, REG[40h] bits 3-1 = 001b.

bits 3-2 Transparency Select bits [1:0]

These bits select the transparency mode.

Normal Mode: in this mode, if the resulting scaled pixels equal the transparent color, they are not written to memory. In this mode, there will be color artifacts surrounding the non-transparent color.

Black/White Mode: in this mode, the transparent color is limited to white or black with the visible color being the opposite. In this mode, color artifacts are removed by forcing all pixels to be either transparent or not.

Text Mode: In this mode, the transparent color intensity range calculated from the Transparency Color Registers (REG[98h] ~ REG[9Ch]) determines if the pixel is transparent or not. This mode is similar to Black/White mode with the effect of removing more color artifacts.

Table 11-22: Transparency Select

REG[62h] bits 3-2	Transparency Mode
00b (default)	Disabled
01b	Normal Mode
10b	Black/White Mode
11b	Text Mode

bits 1-0 Window Rotation bits [1:0]

These bits determine the counter clock wise rotation applied to the window being written. If writing data from the Host, setting these bits will rotate as appropriate.

Table 11-23: Window Rotation

REG[6Ah] bits 1-0	Window Rotation
00b (default)	0°
01b	90°
10b	180°
11b	270°

Input Window Size / Position Registers

All windows written from the Host require the following parameters:

- Input Size (height, width): If processing the Background Image, the input size combined with the double-buffer bit is used to determine the scale-down ratio required to fit the image within available memory. All destructive windows written on-top of the background use the same scale-down ratio as the original background image.
- Output Size (height, width): If processing the Background Image, the Output Size is used to determine the scale-up ratio. All destructive windows written on-top of the background use the same scale-up ratio as the original background image.
- Output Position (only applicable if displaying multiple windows): The original Background Image does not have an associated position as it is always centered and bordered (if necessary). All destructive windows are referenced to the top-left of the background image.
- Background or Destructive Overlay?
- Double-Buffered?

Limitations

If the Double-Buffer feature is disabled, then there is 312k bytes of memory available for the image. If the Double-Buffer feature is enabled, then there is 156k bytes of memory available for the image.

The maximum input window resolution for RGB and YUV 4:2:2 formats is 3072x4092. The maximum input window resolution for YUV 4:2:0 format is 720x4092.

The overlay window output x,y start positions are referenced to the background output size (size after scaling). The overlay input window size is referenced to the background input size (size before scaling).

Depending on the background input window resolution, the input window width must be divisible by 2, 4, or 8, and height must be divisible by 2, 4, or 8. All subsequent destructive windows must follow the same divisibility numbers as the background window. The input window width/height divisibility thresholds are as follows:

Table 11-24: Window Width/Height Divisibility Thresholds

If either input width or height is within the range:		Both Restrictions Apply	
Input Window Width	**Input Window Height**	**Width Divisible by**	**Height Divisible by**
2 ƒ width ƒ 768	2 ƒ height ƒ1022	2	2
772 ƒ width ƒ 1536	1024 ƒ height ƒ2044	4	4
1544 ƒ width ƒ 3072	2048 ƒ height ƒ 4088	8	8

Note

1. In cases where the width and height fall within 2 different ranges with different divisibility restrictions, the largest divisibility restriction applies to both width and height. For example, a 720x2048 window has divisibility restrictions of 8 for both width and height.
2. When either the input width or input height falls within the ranges listed below, the associated restriction must be observed.
   a. If 2 ƒ width ƒ 768 or 2 ƒ height ƒ 1022, the following restriction applies:
      Input Width x Input Height ≤ 524,288
   2. For 772 ƒ width ƒ 1536 or 1024 ƒ Height ƒ 2044, the following restriction applies:
      Input Width ‰ 2 x Input Height ‰ 2 ≤ 524,288
   3. For 1544 ƒ width ƒ 3072 or 2048 ƒ Height ƒ 4088, the following restriction applies:
      Input Width ‰ 4 x Input Height ‰ 4 ≤ 524,288

The following figure indicates supported input image resolutions as colored regions. Gray areas indicate background window resolutions that are not supported. The curves defining the bottom boundaries of not supported resolutions are defined as:

Lower Gray Area
Height = A ‰ Width, where A = 524288
Upper Gray Area
Height = A ‰ Width, where A = 2097152
Upper Boundary
Height = A ‰ Width, where A = 8388608

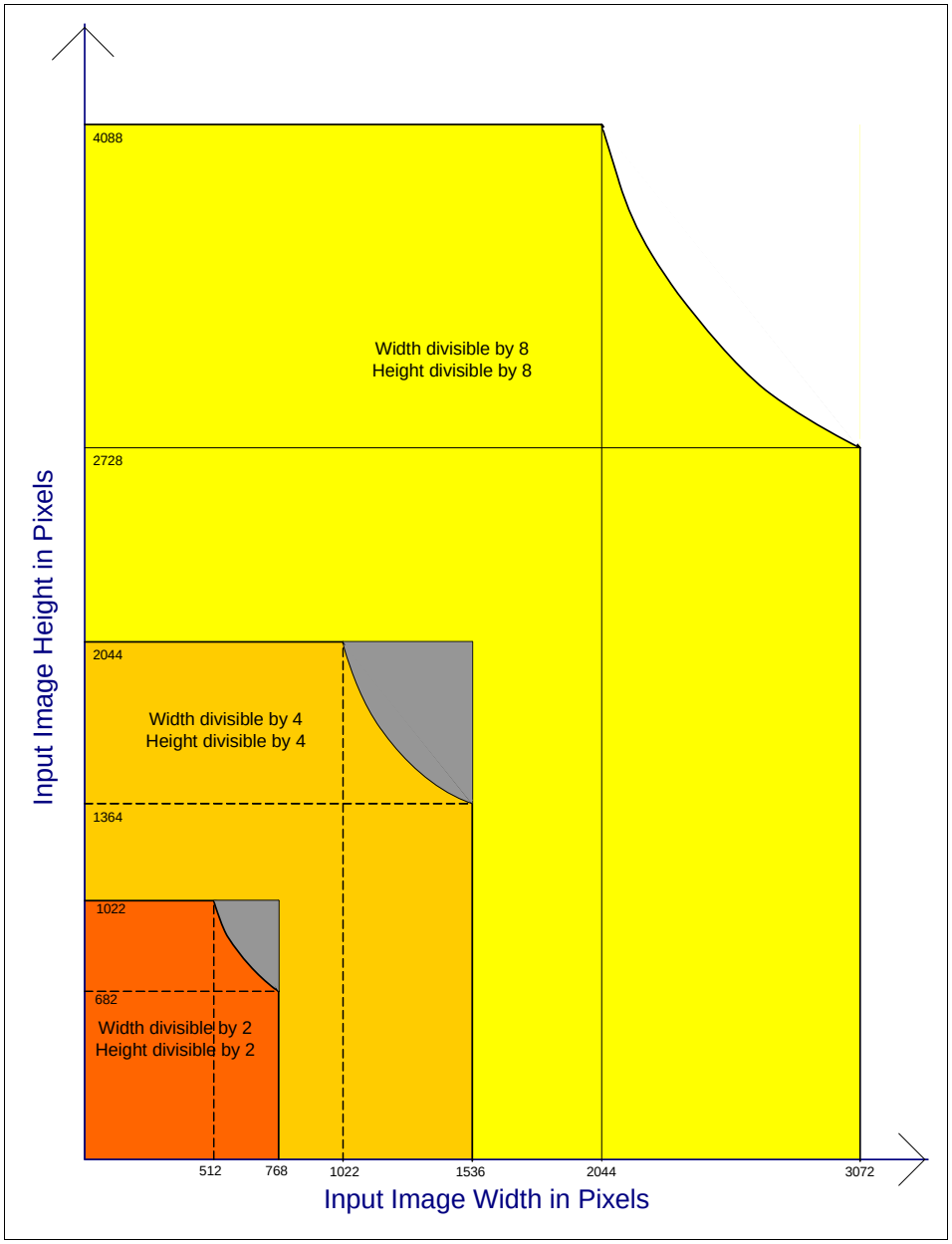


Figure 11-1: Input Image Restrictions Summary

The following table provides typical supported panel resolutions.

Figure 11-2: Example Supported Input Sizes

Example Common Supported Input Sizes	Resolution
QCIF	176x144
QVGA	320x240
CIF	352x288
WQVGA	400x240
VGA	640x480
WVGA	800x480
SVGA	800x600
XGA	1024x768
Wide Screen XGA	1280x800
SXGA	1280x1024
WXGA+	1440x900
UXGA	1600x1200
WUXGA+	2560x1600
720p	1280X720
1080i/p	1920X1080
1080p	1920x1080

REG[64h] Host Input Window Height Register 0
Default = 00h Read/Write

Host Input Window Height bits 7-0							
7	6	5	4	3	2	1	0

REG[66h] Host Input Window Height Register 1
Default = 00h Read/Write

n/a				Host Input Window Height bits 11-8			
7	6	5	4	3	2	1	0

REG[66h] bits 3-0
REG[64h] bits 7-0 Host Input Window Height bits [11:0]
These bits determine the height of the window input from the Host, in pixels. This value should specify the height of the input image prior to applying rotation.

REG[68h] Host Input Window Width Register 0
Default = 00h Read/Write

Host Input Window Width bits 7-0							
7	6	5	4	3	2	1	0

REG[6Ah] Host Input Window Width Register 1
Default = 00h Read/Write

n/a				Host Input Window Width bits 11-8			
7	6	5	4	3	2	1	0

REG[6Ah] bits 3-0
REG[68h] bits 7-0 Host Input Window Width bits [11:0]
These bits determine the width of the window input from the Host, in pixels. This value should specify the width of the input image prior to applying rotation.

11.3.5 Display Output Control Registers

REG[80h] Display Mode Register							
Default = 00h							Read/Write
Macrovision Enable	n/a			TV Display Blank	TV Enable	n/a	
7	6	5	4	3	2	1	0

bit 7 Macrovision Enable
The Macrovision feature is a bond out option on the S1D13746. Therefore, Macrovision can only be enabled when the Macrovision Bond Option bit is set to 1b, REG[02h] bit 7 = 1b. When REG[02h] bit 7 = 0b, this bit has no effect.
When this bit = 0b, the Macrovision block is enabled.
When this bit = 1b, the Macrovision block is disabled.

bit 3 TV Display Blank
This bit controls the TV display pipeline and allows the TV display to be “blanked”.
When this bit = 0b, the TV display pipeline is enabled.
When this bit = 1b, all TV data outputs are forced to zero (i.e. the screen is blanked).

bit 2 TV Enable
This bit controls the TV interface.
When this bit = 0b, the TV interface is disabled and all TV control signals are inactive.
When this bit = 1b, the TV interface is enabled.

Display Output Window Size / Position Registers

When writing a single or background image (REG[62h] bit 5), the desired Output Width / Height are required. The start position must be programmed to 0.

When writing destructive overlays (multiple windows), only the Start position is necessary. The Start position of the overlay window is relative to the top-left of the displayed background image.

Note

The overlay window output x,y start positions are referenced to the background output size (size after scaling). The overlay input window size is referenced to the background input size (size before scaling).

REG[82h] Display Output Window X Start Position Register 0

Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Display Output Window X Start Position bits 7-0							

REG[84h] Display Output Window X Start Position Register 1

Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Display Output Window X Start Position bits 9-8	

REG[84h] bits 1-0
REG[82h] bits 7-0 Display Output Window X Start Position bits [9:0]

These bits determine the X start position of the window in relation to the top left corner of the background image, in pixels. For rotated orientations (see REG[62h] bits 1-0), the top left corner is still relative to the displayed image.

Note

If the host is writing the background image, these bits must be set to zero.

REG[86h] Display Output Window Y Start Position Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
Display Output Window Y Start Position bits 7-0							

REG[88h] Display Output Window Y Start Position Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						Display Output Window Y Start Position bits 9-8	

REG[88h] bits 1-0
REG[86h] bits 7-0 Display Output Window Y Start Position bits [9:0]
These bits determine the Y start position of the window in relation to the top left corner of the background image, in pixels. For rotated orientations (see REG[62h] bits 1-0), the top left corner is still relative to the displayed image.

Note
If the host is writing the background image, these bits must be set to zero.

REG[8Ah] Display Output Window Height Register 0
Default = 40h Read/Write

7	6	5	4	3	2	1	0
Display Output Window Height bits 7-0							

REG[8Ch] Display Output Window Height Register 1
Default = 02h Read/Write

7	6	5	4	3	2	1	0
n/a						Display Output Window Height bits 9-8	

REG[8Ch] bits 1-0
REG[8Ah] bits 7-0 Display Output Window Height bits [9:0]
These bits determine the height of the window output to the display, in pixels. This value is used to determine the ratio required to scale-up the image stored in memory to the resulting displayed image. For rotated orientations (see REG[62h] bits 1-0), the top left corner is still relative to the displayed image.

Note
1. These bits are only used for the initial background image. All subsequent windows use the same scale ratio as defined by the background image.
2. The values of these registers are latched when REG[90h] is written, during the TV Vertical Blanking Period. REG[90h] should be the last register written before writing image data.

REG[8Eh] Display Output Window Width Register 0
Default = D0h Read/Write

Display Output Window Width bits 7-0							
7	6	5	4	3	2	1	0

REG[90h] Display Output Window Width Register 1
Default = 02h Read/Write

n/a						Display Output Window Y End Position bits 9-8	
7	6	5	4	3	2	1	0

REG[90h] bits 1-0
REG[8Eh] bits 7-0 Display Output Window Width bits [9:0]

These bits determine the with of the output window to the display, in pixels. This value is used to determine the scale-up ratio from the image stored in memory to the resulting displayed image. For rotated orientations (see REG[62h] bits 1-0), the top left corner is still relative to the displayed image.

Note

1. These bits are only used for the initial background image. All subsequent windows use the same scale ratio as defined by the background image.
2. When writing a background image, the values of these registers are latched when REG[90h] is written, during the TV Vertical Blanking Period. REG[90h] should be the last register written before writing image data.

Border Color Registers

REG[92h] Border Color Register 0
Default = 10h — Read/Write

7	6	5	4	3	2		
Border Color - Y [7:0]							

REG[94h] Border Color Register 1
Default = 80h — Read/Write

7	6	5	4	3	2		
Border Color - U [7:0]							

REG[96h] Border Color Register 2
Default = 80h — Read/Write

7	6	5	4	3	2	1	0
Border Color - V [7:0]							

REG[96h] bits 7-0 Border Color - V [7:0]
REG[94h] bits 7-0 Border Color - U [7:0]
REG[92h] bits 7-0 Border Color - Y [7:0]

These bits specify the YUV (8:8:8) components of the border color which is used if the resulting output TV resolution does not match the appropriate full-screen resolution of the selected display format (PAL or NTSC). When this occurs, the Display Output Window is automatically centered within a border of the specified color.

The border color must be set to a value within the YCbCr Offset range as shown below.

$16 \leq Y \leq 235$
$16 \leq U \leq 240$
$16 \leq V \leq 240$

To calculate the YUV values for an equivalent RGB color, use the following formulas.

Y = (838h x R + 1022h x G + 322h x B) ‰ 2000h + 10h
U = (-4C1h x R - 94Eh x G + E0Eh x B) ‰ 2000h + 80h
V = (E0Eh x R - BC7h x G - 247h x B) ‰ 2000h + 80h

Transparency Color Registers

REG[98h] TV Transparency Color Register 0
Default = 10h — Read/Write

Transparency Color - Y [7:0]							
7	6	5	4	3	2	1	0

REG[9Ah] TV Transparency Color Register 1
Default = 80h — Read/Write

Transparency Color - U [7:0]							
7	6	5	4	3	2	1	0

REG[9Ch] TV Transparency Color Register 2
Default = 80h — Read/Write

Transparency Color - V [7:0]							
7	6	5	4	3	2	1	0

REG[9Ch] bits 7-0 Transparency Color - V [7:0]
REG[9Ah] bits 7-0 Transparency Color - U [7:0]
REG[98h] bits 7-0 Transparency Color - Y [7:0]

These bits specify the YUV (8:8:8) components of the transparency color. Transparency can only be used during the host data write. In this case, the transparency color is stripped from the input data before being written to memory, and therefore once written (enabled) can not be disabled. As with all other windows written, the transparency window is also considered destructive and can not be un-done.

The transparency color must be set to a value within the YCbCr Offset range as shown below, even if the input image data is in a different format.

$16 \leq Y \leq 235$
$16 \leq U \leq 240$
$16 \leq V \leq 240$

To calculate the YUV values for an equivalent RGB color, use the following formulas.

Y = (838h x R + 1022h x G + 322h x B) ‰ 2000h + 10h
U = (-4C1h x R - 94Eh x G + E0Eh x B) ‰ 2000h + 80h
V = (E0Eh x R - BC7h x G - 247h x B) ‰ 2000h + 80h

REG[9Eh] DAC Reference Source Select Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
TV Display Horizontal Direction	TV Display Horizontal Position bits 2-0			TV Display Vertical Position bits 1-0		IREF Enable	VREF Enable

bit 7 TV Display Horizontal Direction
This bit controls the direction the TV display moves when the TV Display Horizontal Position (REG[9Eh] bits 6-4) is set.
When this bit = 0b, REG[9Eh] bits 6-4 set the number of pixels the TV display will move to the left.
When this bit = 1b, REG[9Eh] bits 6-4 set the number of pixels the TV display will move to the right.

bits 6-4 TV Display Horizontal Position bits [2:0]
These bits set the TV display horizontal position offset, in pixels, from the default position. The direction of the offset is controlled with bit 7 of this register.

bits 3-2 TV Display Vertical Position bits [1:0]
These bits set the number of lines the TV display is moved down from the default position.

bit 1 IREF Enable
DAC reference current source circuit enable.
When this bit = 0b, the internal generation of the reference current is disabled. (Default)
When this bit = 1b, the VADJ pin is enabled. For more information see Section 24.1, “DAC External Components” on page 184

bit 0 VREF Enable
DAC reference voltage source circuit enable.
When this bit = 0b, the DAC uses the external VREF mode. See “DAC External Components” on page 184.(Default)
When this bit = 1b, the DAC uses the internal VREF mode. In this mode, the DAC reference voltage is supplied by the DAC.

11.3.6 Display Memory Access Registers

REG[A0h] Display Memory Data Port Register 0
Default = not applicable — Read/Write

Display Memory Data Port bits 15-8							
7	6	5	4	3	2	1	0
Display Memory Data Port bits 7-0							
7	6	5	4	3	2	1	0

REG[A0h] bits 15-0 Display Memory Data Port bits [15:0]
These bits are the data port for Host data writes to display memory and are used for all configurations.

Bits 7-0 form the least significant byte of the data word and are used for both 8-bit accesses (CNF[1:0] = 01b) and 16-bit accesses (CNF[1:0] = 11b). Bits 15-8 form the most significant byte of the data word and are used only for 16-bit accesses (CNF[1:0] = 11b).

Note

1. Burst data writes are supported through these registers. Once reaching this address, register auto increment is automatically disabled and all further writes to this register auto increment the internal memory address only.
2. The Host Window Size / Position registers (REG[64h] ~ REG[6Ah], REG[82h] ~ REG[88h]) must be programmed prior to writing the data.

REG[A2h] through REG[A6h] are Reserved

These registers are reserved and must not be written.

11.3.7 3X3 Pixel Matrix Filter Registers

REG[C0h] 3X3 Pixel Matrix Filter Control Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a							3x3 Filter Enable

bit 0 3x3 Filter Enable
This bit enables the 3x3 Filter. See Section 16, “Image Enhancement Engine” on page 140 for further information.
When this bit = 0b, the 3x3 Filter is disabled.
When this bit = 1b, the 3x3 Filter is enabled.

Note
SYSCLK must be 54MHz when 3x3 filter is enabled

3X3 Pixel Matrix Filter Coefficient Registers

Table 11-25: Coefficient Table Mapping

Coefficient Table #	Register Address	Use for 3x3 Filter
0	REG[C2h] bits 2-0	Y0
1	REG[C2h] bits 6-4	Y1
2	REG[C4h] bits 2-0	Y2
3	REG[C4h] bits 6-4	Y3
4	REG[C6h] bits 4-0	Y4
5	REG[C8h] bits 2-0	Y5
6	REG[C8h] bits 6-4	Y6
7	REG[CAh] bits 2-0	Y7
8	REG[CAh] bits 6-4	Y8
9	REG[CCh] bits 2-0	U0
10	REG[CCh] bits 6-4	U1
11	REG[CEh] bits 2-0	U2
12	REG[CEh] bits 6-4	U3
13	REG[D0h] bits 4-0	U4

Coefficient Table #	Register Address	Use for 3x3 Filter
14	REG[D2h] bits 2-0	U5
15	REG[D2h] bits 6-4	U6
16	REG[D4h] bits 2-0	U7
17	REG[D4h] bits 6-4	U8
18	REG[D6h] bits 2-0	V0
19	REG[D6h] bits 6-4	V1
20	REG[D8h] bits 2-0	V2
21	REG[D8h] bits 6-4	V3
22	REG[DAh] bits 4-0	V4
23	REG[DCh] bits 2-0	V5
24	REG[DCh] bits 6-4	V6
25	REG[DEh] bits 2-0	V7
26	REG[DEh] bits 6-4	V8

Y0	Y3	Y6
Y1	Y4	Y7
Y2	Y5	Y8

U0	U3	U6
U1	U4	U7
U2	U5	U8

V0	Y3	V6
V1	Y4	V7
V2	V5	V8

Figure 11-3: YUV Coefficient Matrix

Note

The data range for each coefficient is -15 to 15 (decimal) for the middle pixel and -3 to 3 (decimal) for all others. The two's complement values must be set from 10h to 0Fh.
For Y4, U4, V4 the data range for the coefficients is -16 to 15. The 2's compliment values must be set from 10h to 0Fh. For all other coefficients, the data range is -4 to 3. The 2's compliment values must be set from 4h to 3h.

Note

The Y data after 3x3 filtering is:
$Y' = (Y_0C_0+Y_1C_1+Y_2C_2+Y_3C_3+Y_4C_4+Y_5C_5+Y_6C_6+Y_7C_7+Y_8C_8) / Scale + Offset$
Scale: REG[E0h]
Offset: REG[E6h]
$C_{0\sim8}$: Coefficient (REG[C2h] ~ REG[CAh])
$Y_{0\sim8}$: Original Y data
$Y_0\ Y_3\ Y_6$
$Y_1\ Y_4\ Y_7$
$Y_2\ Y_5\ Y_8$

Note

The U data after 3x3 filtering is:
$U' = (U_0C_9+U_1C_{10}+U_2C_{11}+U_3C_{12}+U_4C_{13}+U_5C_{14}+U_6C_{15}+U_7C_{16}+U_8C_{17}) / Scale + Offset$
Scale: REG[E2h]
Offset: REG[E8h]
$C_{9\sim17}$: Coefficient (REG[CCh] ~ REG[D4h])
$U_{0\sim8}$: Original U data
$U_0\ U_3\ U_6$
$U_1\ U_4\ U_7$
$U_2\ U_5\ U_8$

Note

The V data after 3x3 filtering is:
$V' = (V_0C_{18}+V_1C_{19}+V_2C_{20}+V_3C_{21}+V_4C_{22}+V_5C_{23}+V_6C_{24}+V_7C_{25}+V_8C_{26}) / Scale + Offset$
Scale: REG[E4h]
Offset: REG[EAh]
$C_{18\sim26}$: Coefficient (REG[D6h] ~ REG[DEh])
$V_{0\sim8}$: Original V data
$V_0\ V_3\ V_6$
$V_1\ V_4\ V_7$
$V_2\ V_5\ V_8$

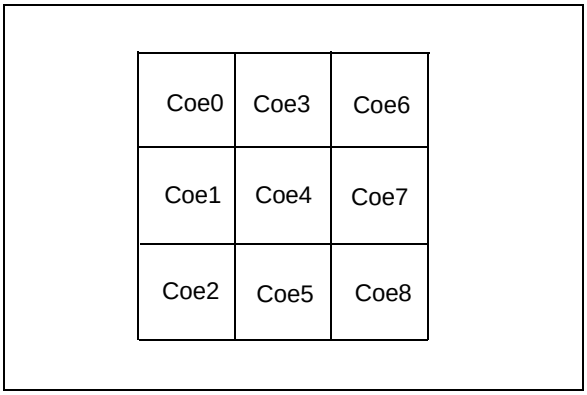


Figure 11-4 Coefficient Matrix

The filter scans left to right, top to bottom, with coe4 multiplying by the current pixel. The coefficients operate on each YUV component separately. After scaling and offsets are applied, the value is clipped back to 16 to 235 for the Y component and 16 to 240 for the U and V components.

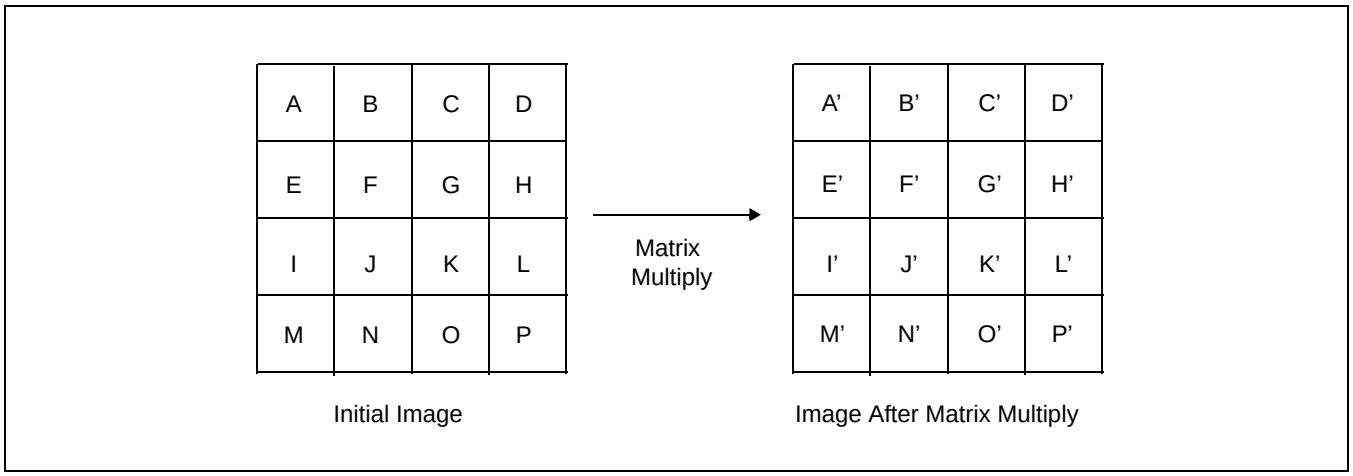


Figure 11-5 Matrix Multiply Example

The following formulas are used to calculate the resulting components (F'y, F'u, F'v). F is the pixel used in the calculation and the component sizes are Fy (8 bits), Fu (8 bits), and Fv (8 bits).

F'y = Ay * Coe0 + By * Coe3 + Cy * Coe6 + Ey * Coe1 + Fy * Coe4 + Gy * Coe7 + Iy * Coe2 + Jy * Coe5 + Ky * Coe8
F'u = Au * Coe0 + Bu * Coe3 + Cu * Coe6 + Eu * C0e1 + Fu * Coe4 + Gu * Coe7 + Iu * Coe2 + Ju * Coe5 + Ku * Coe8
F'v = Av * Coe0 + Bv * Coe3 + Cv * Coe6 + Ev * C0e1 + Fv * Coe4 + Gv * Coe7 + Iv * Coe2 + Jv * Coe5 + Kv * Coe8

The top/left/right/bottom edges and corners of the original image are treated as follows, when the 3x3 matrix is applied to the edges and corners.

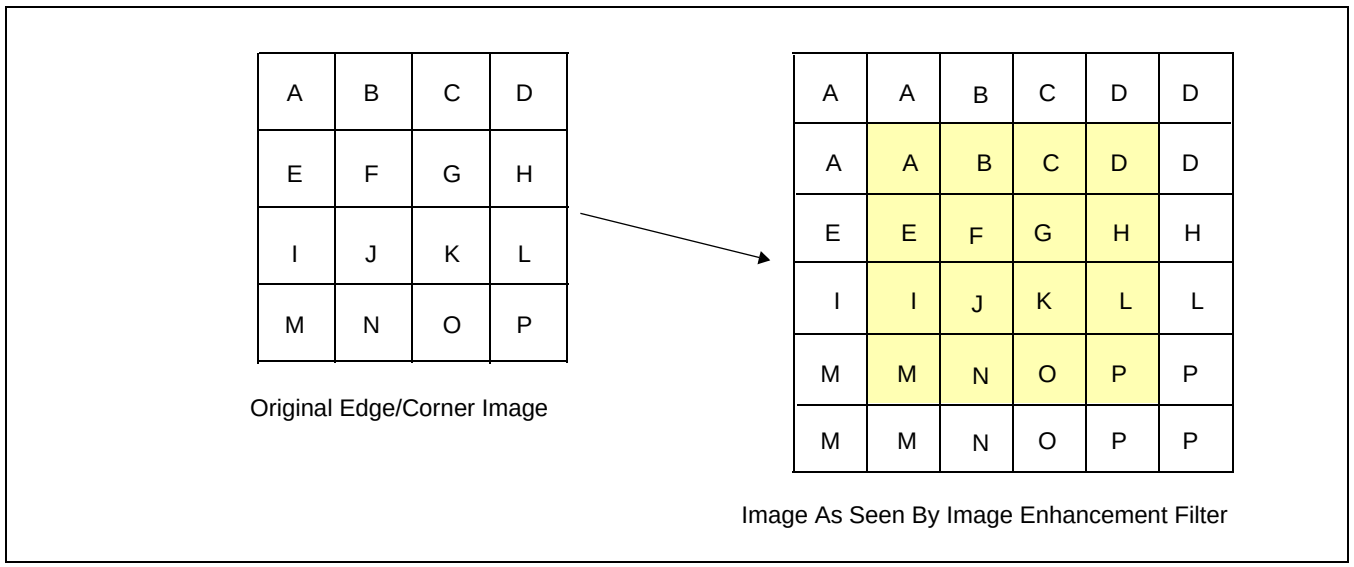


Figure 11-6 Edge/Corner Adjustment

The following formulas are used to calculate the resulting components (F'y, F'u, F'v). A is the pixel used in the calculation and the component sizes are Ay (8 bits), Au (8 bits), and Av (8 bits).

A'y = Ay * Coe0 + Ay * Coe3 + By * Coe6 + Ay * C0e1 + Ay * Coe4 + By * Coe7 + Ey * Coe2 + Ey * Coe5 + Fy * Coe8
A'u = Au * Coe0 + Au * Coe3 + Bu * Coe6 + Au * C0e1 + Au * Coe4 + Bu * Coe7 + Eu * Coe2 + Eg* Coe5 + Fu * Coe8
A'v = Av * Coe0 + Av * Coe3 + Bv * Coe6 + Av * C0e1 + Av * Coe4 + Bv * Coe7 + Ev * Coe2 + Eb* Coe5 + Fv * Coe8

REG[C2h] 3X3 Pixel Matrix Filter Coefficient Table Register 0
Default = 00h — Read/Write

n/a	Y1 Coefficient Table bits 2-0			n/a	Y0 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 Y1 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 Y0 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[C4h] 3X3 Pixel Matrix Filter Coefficient Table Register 1
Default = 00h Read/Write

n/a	Y3 Coefficient Table bits 2-0			n/a	Y2 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 Y3 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 Y2 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[C6h] 3X3 Pixel Matrix Filter Coefficient Register 2
Default = 01h Read/Write

n/a			Y4 Coefficient Table bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 Y4 Coefficient Table bits [4:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[C8h] 3X3 Pixel Matrix Filter Coefficient Table Register 3
Default = 00h Read/Write

n/a	Y6 Coefficient Table bits 2-0			n/a	Y5 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 Y6 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 Y5 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[CAh] 3X3 Pixel Matrix Filter Coefficient Table Register 4
Default = 00h Read/Write

n/a	Y8 Coefficient Table bits 2-0			n/a	Y7 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 Y8 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 Y7 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[CCh] 3X3 Pixel Matrix Filter Coefficient Table Register 5
Default = 00h Read/Write

n/a	U1 Coefficient Table bits 2-0			n/a	U0 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 U1 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 U0 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[CEh] 3X3 Pixel Matrix Filter Coefficient Table Register 6
Default = 00h Read/Write

n/a	U3 Coefficient Table bits 2-0			n/a	U2 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 U3 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 U2 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[D0h] 3X3 Pixel Matrix Filter Coefficient Register 7
Default = 01h Read/Write

n/a			U4 Coefficient Table bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 U4 Coefficient Table bits [4:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[D2h] 3X3 Pixel Matrix Filter Coefficient Table Register 8
Default = 00h Read/Write

n/a	U6 Coefficient Table bits 2-0			n/a	U5 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 U6 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 U5 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[D4h] 3X3 Pixel Matrix Filter Coefficient Table Register 9
Default = 00h Read/Write

n/a	U8 Coefficient Table bits 2-0			n/a	U7 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 U8 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 U7 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[D6h] 3X3 Pixel Matrix Filter Coefficient Table Register 10
Default = 00h Read/Write

n/a	V1 Coefficient Table bits 2-0			n/a	V0 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 V1 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 V0 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[D8h] 3X3 Pixel Matrix Filter Coefficient Table Register 11
Default = 00h Read/Write

n/a	V3 Coefficient Table bits 2-0			n/a	V2 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 V3 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 V2 Coefficient Table f bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[DAh] 3X3 Pixel Matrix Filter Coefficient Register 12
Default = 01h Read/Write

n/a			V4 Coefficient Table bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 V4 Coefficient Table bits [4:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[DCh] 3X3 Pixel Matrix Filter Coefficient Table Register 13
Default = 00h Read/Write

n/a	V6 Coefficient Table bits 2-0			n/a	V5 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 V6 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 V5 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[DEh] 3X3 Pixel Matrix Filter Coefficient Table Register 14
Default = 00h Read/Write

n/a	V8 Coefficient Table bits 2-0			n/a	V7 Coefficient Table bits 2-0		
7	6	5	4	3	2	1	0

bits 6-4 V8 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

bits 2-0 V7 Coefficient Table bits [2:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b). These signed 2's complement values specify the coefficient tables for the filter and are arranged **Vertically**.

REG[E0h] 3X3 Pixel Matrix Filter Scale Value for Luminance Y Channel Register
Default = 01h Read/Write

n/a		Filter Scale Value for Luminance Y Channel bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 Filter Scale Value for Luminance Y Channel bits [5:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b) and are ignored for all other operations. These unsigned bits specify the filter scale value for luminance (Y channel) and must be programmed such that the following formula is valid.

1 ƒ REG[E0h] bits 5-0 ƒ 3Fh

REG[E2h] 3X3 Pixel Matrix Filter Scale Value for Chrominance U Channel Register
Default = 01h Read/Write

n/a		Filter Scale Value for Chrominance U Channel bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 Filter Scale Value for Chrominance U Channel bits [5:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b) and are ignored for all other operations. These unsigned bits specify the filter scale value for chrominance (U channel) and must be programmed such that the following formula is valid.

1 ƒ REG[E2h] bits 5-0 ƒ 3Fh

REG[E4h] 3X3 Pixel Matrix Filter Scale Value for Chrominance V Channel Register
Default = 01h Read/Write

n/a		Filter Scale Value for Chrominance V Channel bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 Filter Scale Value for Chrominance V Channel bits [5:0]
These bits are only used when the filter operation is selected (REG[C0h] bit 0 = 1b) and are ignored for all other operations. These unsigned bits specify the filter scale value for chrominance (V channel) and must be programmed such that the following formula is valid.

1 ƒ REG[E4h] bits 5-0 ƒ 3Fh

REG[E6h] 3X3 Pixel Matrix Filter Offset Value for Luminance Y Channel Register
Default = 00h Read/Write

Filter Offset Value for Luminance Y Channel bits 8-1							
7	6	5	4	3	2	1	0

bits 7-0 Filter Offset Value for Luminance Y Channel bits [8:1]
This register is only used when the filter operation is selected (REG[C0h] bit 0 = 1b) and are ignored for all other operations. This register specifies bits [8:1] of the desired offset value (bit 0 is internal and forced to 0). These signed 2's complement bits specify the filter offset value for luminance (Y channel).

Note
The data range for each offset is -256 to 254 (decimal). The two's complement values must be set from 10h to 7Fh. For example, if an offset of 42h is required, program this register with 21h.

REG[E8h] 3X3 Pixel Matrix Filter Offset Value for Chrominance U Channel Register
Default = 00h Read/Write

Filter Offset Value for Chrominance U Channel bits 8-1							
7	6	5	4	3	2	1	0

bits 7-0 Filter Offset Value for Chrominance U Channel bits [8:1]
This register is only used when the filter operation is selected (REG[C0h] bit 0 = 1b) and are ignored for all other operations. This register specifies bits [8:1] of the desired offset value (bit 0 is internal and forced to 0). These signed 2's complement bits specify the filter offset value for chrominance (U channel).

Note
The data range for each offset is -256 to 254 (decimal). The two's complement values must be set from 10h to 7Fh. For example, if an offset of 42h is required, program this register with 21h.

REG[EAh] 3X3 Pixel Matrix Filter Offset Value for Chrominance V Channel Register
Default = 00h Read/Write

Filter Offset Value for Chrominance V Channel bits 8-1							
7	6	5	4	3	2	1	0

bits 7-0 Filter Offset Value for Chrominance V Channel bits [8:1]
This register is only used when the filter operation is selected (REG[C0h] bit 0 = 1b) and are ignored for all other operations. This register specifies bits [8:1] of the desired offset value (bit 0 is internal and forced to 0). These signed 2's complement bits specify the filter offset value for chrominance (V channel).

Note
The data range for each offset is -256 to 254 (decimal). The two's complement values must be set from 10h to 7Fh. For example, if an offset of 42h is required, program this register with 21h.

11.3.8 Miscellaneous Registers

REG[ECh] Non-Display Period Control / Status Register
Default = 26h — Read/Write

7	6	5	4	3	2	1	0
n/a		TE Status (RO)	Input Busy Status (RO)	TE Output Pin Enable	TE Output Pin Function Select bits 2-0		

bit 5 TE Status
This bit indicates the status of the TE output, even when the TE Output Pin is disabled (REG[ECh] bit 3 = 0b).
When this bit = 0b, the TE output is low (0).
When this bit = 1b, the TE output is high (1).

bit 4 Input Busy Status (Read Only)
This bit will be high when the input circuitry is busy writing the current window data to memory. There is some latency between the last pixel of a window written by the Host and this bit going low. When writing back-to-back windows, ensure that this bit returns low before writing the next window.
When this bit = 0b, Host Input Window data is not being written to memory.
When this bit = 1b, Host Input Window data is being written to memory.

bit 3 TE Output Pin Enable
This bit determines whether the state of TE is output on the TE pin. The status of TE is still available using the TE Status bit (REG[ECh] bit 5) even when the TE Output Pin is disabled.
When this bit = 0b, the TE output pin is disabled.
When this bit = 1b, the TE output pin is enabled.

bits 2-0 TE Output Pin Function Select bits [2:0]
These bits select which function is indicated by the TE output pin.

Table 11-26: TE Output Pin Function Selection

REG[ECh] bits 2-0	TE Output Pin Function
000b	Reserved
001b	Field 2 VNDP
010b	Field 1 VNDP
011b ~ 100b	Reserved
101b	TV Horizontal Non-Display Period ORed with TV Vertical Non-Display Period (The TE pin and status are active HIGH to indicate the specified condition is TRUE)
110b (default)	TV Vertical Non-Display Period (The TE pin and status are active HIGH to indicate the specified condition is TRUE)
111b	Reserved

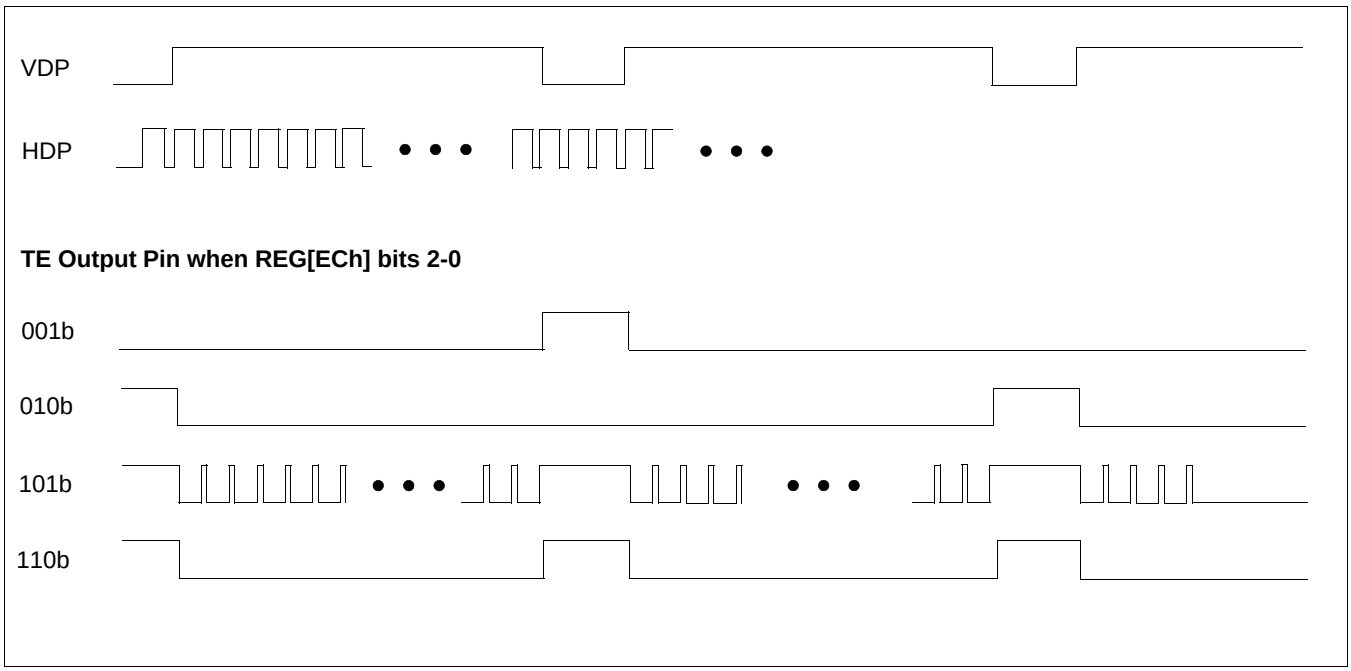


Figure 11-7: TE Output Pin Function Timing

REG[EEh] Parallel RGB Interface Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a				Parallel RGB Interface PCLK Polarity	Parallel RGB Interface HS Polarity	Parallel RGB Interface VS Polarity	Parallel RGB Interface DE Polarity

bit 3 Parallel RGB Interface PCLK Polarity
This bit selects the active polarity of the PCLK signal.
When this bit = 0b, the data is valid on the rising edge of PCLK.
When this bit = 1b, the data is valid on the falling edge of PCLK.

bit 2 Parallel RGB Interface HS Polarity
This bit selects the active polarity of the HS signal.
When this bit = 0b, the data is valid when the HS signal is high.
When this bit = 1b, the data is valid when the HS signal is low.

bit 1 Parallel RGB Interface VS Polarity
This bit selects the active polarity of the VS signal.
When this bit = 0b, the data is valid when the VS signal is high.
When this bit = 1b, the data is valid when the VS signal is low.

bit 0 Parallel RGB Interface DE Polarity
This bit selects the active polarity of the DE signal.
When this bit = 0b, the data is valid when the DE signal is high.
When this bit = 1b, the data is valid when the DE signal is low.

11.3.9 General Purpose IO Pins Registers

REG[F0h] General Purpose IO Pins Configuration Register
Default = 00h — Read/Write

GPIO7 Configuration	GPIO6 Configuration	GPIO5 Configuration	GPIO4 Configuration	GPIO3 Configuration	GPIO2 Configuration	GPIO1 Configuration	GPIO0 Configuration
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Configuration

These bits configure the corresponding GPIO[7:0] pin between an input or output.
When this bit = 0 (normal operation), the corresponding GPIO pin is configured as an input.
When this bit = 1b, the corresponding GPIO pin is configured as an output.

REG[F2h] General Purpose IO Pins Status/Control Register
Default = 00h — Read/Write

GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Status

When the corresponding GPIO[7:0] pin is configured as an output (see REG[F0h]), writing a 1b to this bit drives GPIOx high and writing a 0b to this bit drives GPIOx low.
When the corresponding GPIO[7:0] pin is configured as an input (see REG[F0h]), a read from this bit returns the raw status of GPIOx.

REG[F4h] GPIO Positive Edge Interrupt Trigger Register
Default = 00h — Read/Write

GPIO7 Positive Edge Interrupt Trigger	GPIO6 Positive Edge Interrupt Trigger	GPIO5 Positive Edge Interrupt Trigger	GPIO4 Positive Edge Interrupt Trigger	GPIO3 Positive Edge Interrupt Trigger	GPIO2 Positive Edge Interrupt Trigger	GPIO1 Positive Edge Interrupt Trigger	GPIO0 Positive Edge Interrupt Trigger
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Positive Edge Interrupt Trigger

This bit determines whether the associated GPIO interrupt (see REG[F8h]) is triggered on the positive edge (when the GPIOx pin changes from 0 to 1).
When this bit = 0b, the associated GPIO interrupt (GPIO_INT) is not triggered on the positive edge.
When this bit = 1b, the associated GPIO interrupt (GPIO_INT) is triggered on the positive edge.

REG[F6h] GPIO Negative Edge Interrupt Trigger Register
Default = 00h Read/Write

GPIO7 Negative Edge Interrupt Trigger	GPIO6 Negative Edge Interrupt Trigger	GPIO5 Negative Edge Interrupt Trigger	GPIO4 Negative Edge Interrupt Trigger	GPIO3 Negative Edge Interrupt Trigger	GPIO2 Negative Edge Interrupt Trigger	GPIO1 Negative Edge Interrupt Trigger	GPIO0 Negative Edge Interrupt Trigger
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Negative Edge Interrupt Trigger

This bit determines whether the associated GPIO interrupt (see REG[F8h]) is triggered on the negative edge (when the GPIOx pin changes from 1 to 0).

When this bit = 0b, the associated GPIOx interrupt (GPIO_INT) is not triggered on the negative edge.

When this bit = 1b, the associated GPIOx interrupt (GPIO_INT) is triggered on the negative edge.

REG[F8h] GPIO Interrupt Status Register
Default = 00h Read/Write

GPIO7 Interrupt Status	GPIO6 Interrupt Status	GPIO5 Interrupt Status	GPIO4 Interrupt Status	GPIO3 Interrupt Status	GPIO2 Interrupt Status	GPIO1 Interrupt Status	GPIO0 Interrupt Status
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Interrupt Status

If GPIOs are configured to generate an Interrupt (see REG[F4h] and REG[F6h]), these status bits indicate which GPIO generated the interrupt.

To clear the corresponding GPIO[7:0] Interrupt Status bit, write a 1b then a 0b to the bit.

REG[FAh] GPIO Pull Down Control Register
Default = FFh Read/Write

GPIO7 Pull-down Control	GPIO6 Pull-down Control	GPIO5 Pull-down Control	GPIO4 Pull-down Control	GPIO3 Pull-down Control	GPIO2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Pull-down Control

All GPIO pins have internal pull-down resistors. These bits individually control the state of the corresponding pull-down resistor.

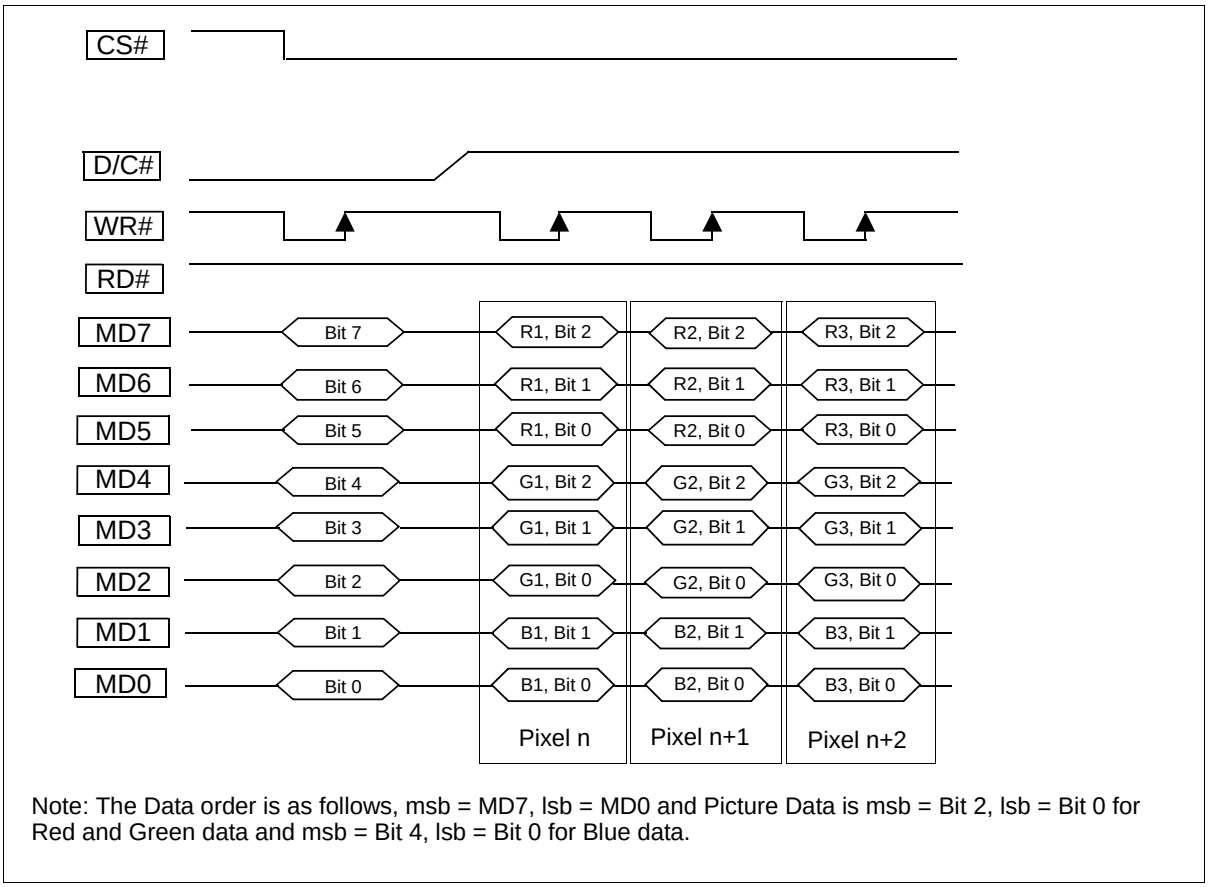
When the bit = 0, the pull-down resistor for the corresponding GPIO pin is inactive.

When the bit = 1, the pull-down resistor for the corresponding GPIO pin is active.

12 Intel 80, 8-Bit Interface Color Formats

12.1 8 bpp Mode (RGB 3:3:2), 256 colors

When REG[60h] bits 3-0 = 0000b and CNF[1:0] = 01, the input data format for the Intel 80 Host interface is RGB 3:3:2.

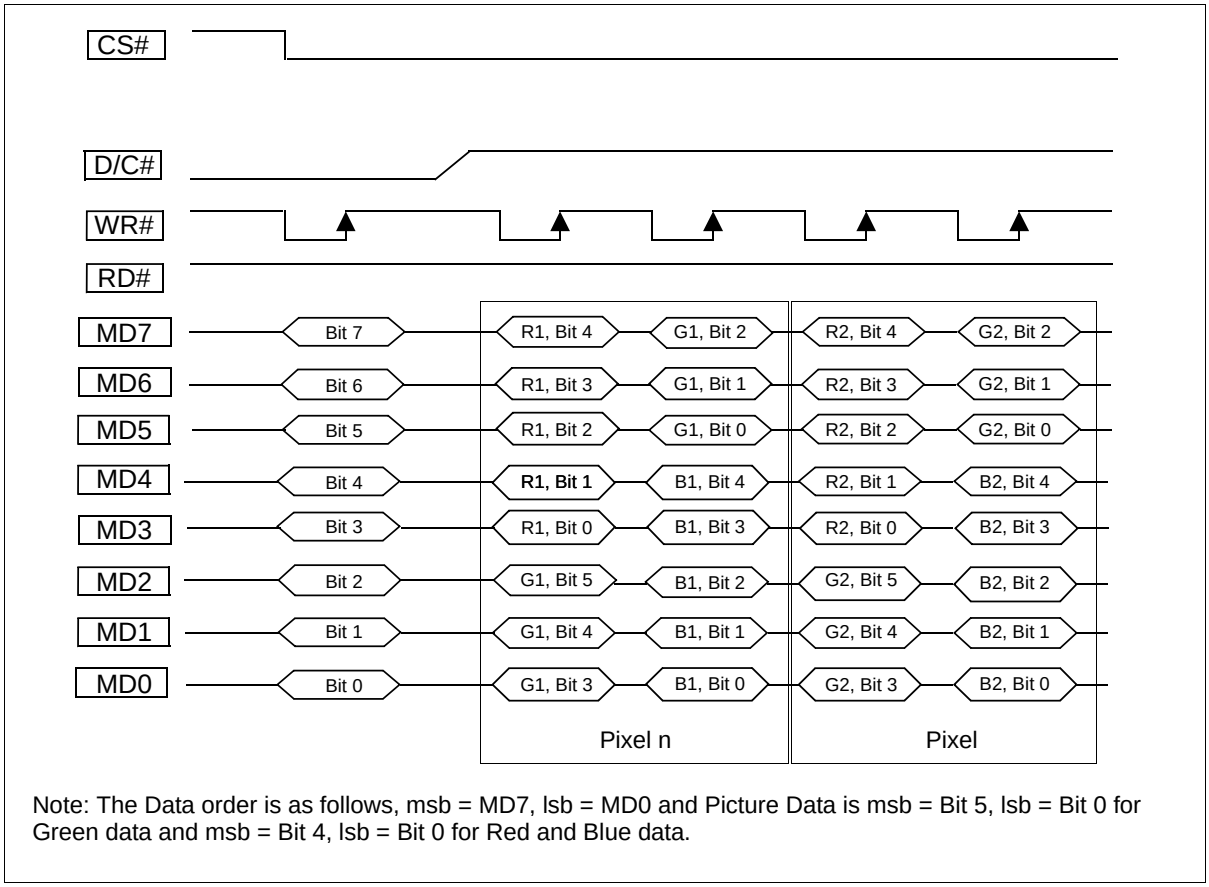


Note: The Data order is as follows, msb = MD7, lsb = MD0 and Picture Data is msb = Bit 2, lsb = Bit 0 for Red and Green data and msb = Bit 4, lsb = Bit 0 for Blue data.

Figure 12-1: 8 bpp Mode (RGB 3:3:2), 256 colors

12.2 16 bpp Mode (RGB 5:6:5), 65,536 colors

When REG[60h] bits 3-0 = 0001b and CNF[1:0] = 01, the input data format for the Intel 80 Host interface is RGB 5:6:5.

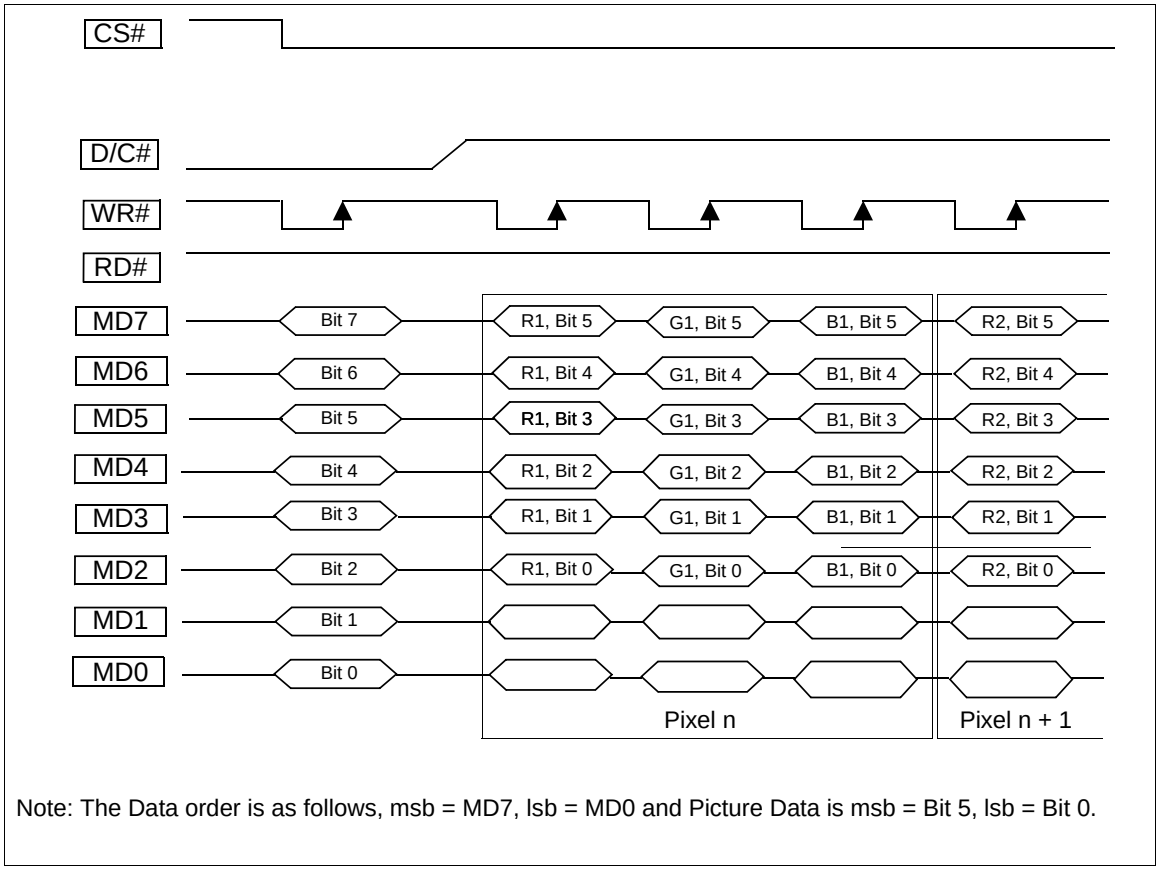


Note: The Data order is as follows, msb = MD7, lsb = MD0 and Picture Data is msb = Bit 5, lsb = Bit 0 for Green data and msb = Bit 4, lsb = Bit 0 for Red and Blue data.

Figure 12-2: 16 bpp Mode (RGB 5:6:5), 65,536 colors

12.3 18 bpp (RGB 6:6:6), 262,144 colors

When REG[60h] bits 3-0 = 0010b and CNF[1:0] = 01, the input data format for the Intel 80 Host interface is RGB 6:6:6.

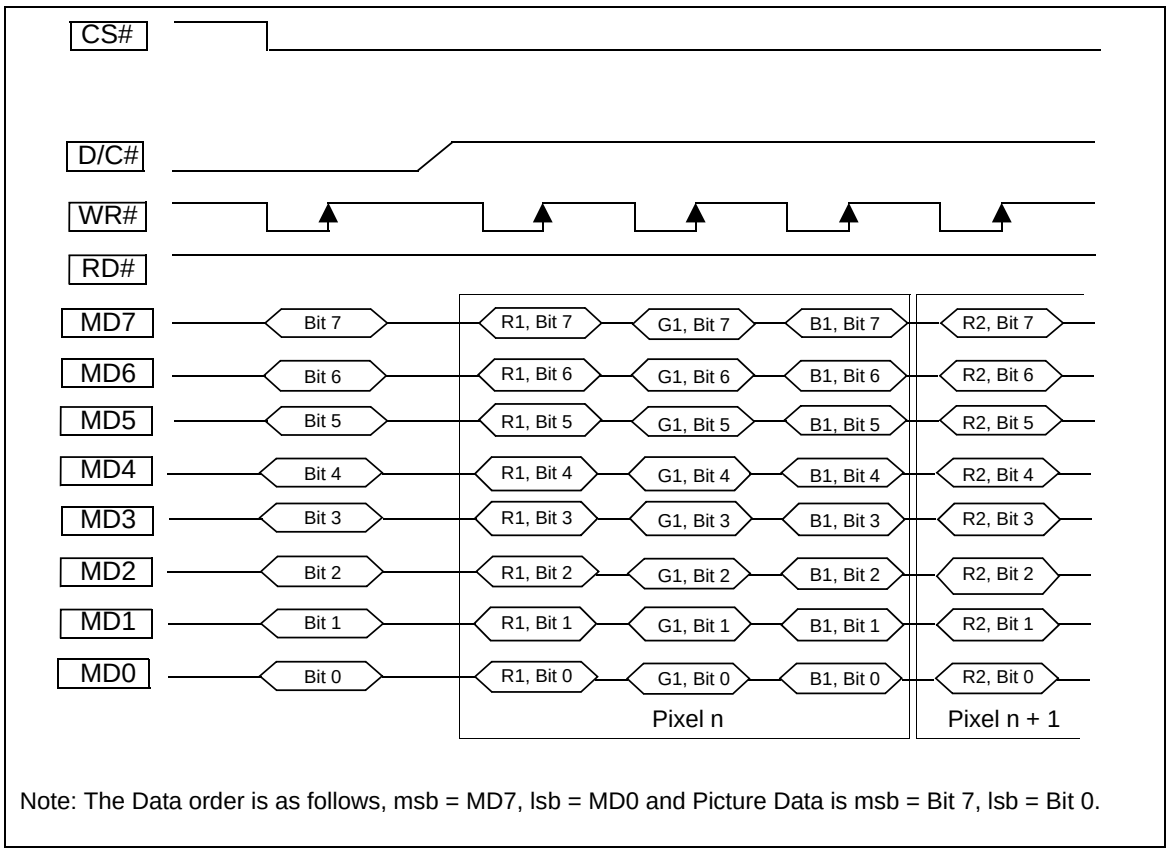


Note: The Data order is as follows, msb = MD7, lsb = MD0 and Picture Data is msb = Bit 5, lsb = Bit 0.

Figure 12-3: 18 bpp (RGB 6:6:6), 262,144 colors

12.4 24 bpp (RGB 8:8:8), 16,777,216 colors

When REG[60h] bits 3-0 = 0011b and CNF[1:0] = 01, the input data format for the Intel 80 Host interface is RGB 8:8:8.



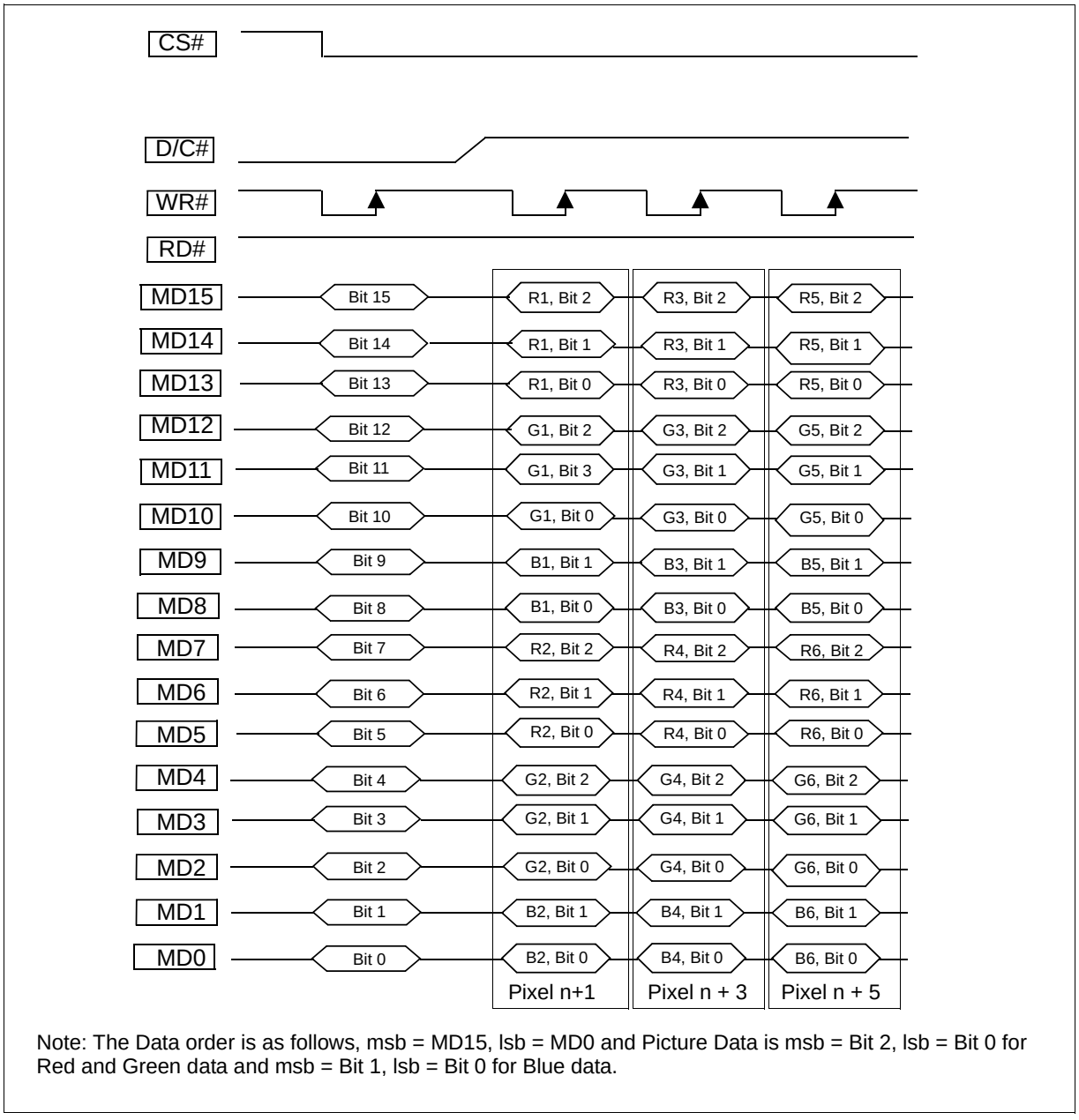
Note: The Data order is as follows, msb = MD7, lsb = MD0 and Picture Data is msb = Bit 7, lsb = Bit 0.

Figure 12-4: 24 bpp (RGB8:8:8), 16,777,216 colors

13 Intel 80, 16-bit Interface Color Formats

13.1 8 bpp (RGB 3:3:2), 256 colors

When REG[60h] bits 3-0 = 0000b and CNF[1:0] = 11, the input data format for the Intel 80 Host interface is RGB 3:3:2.

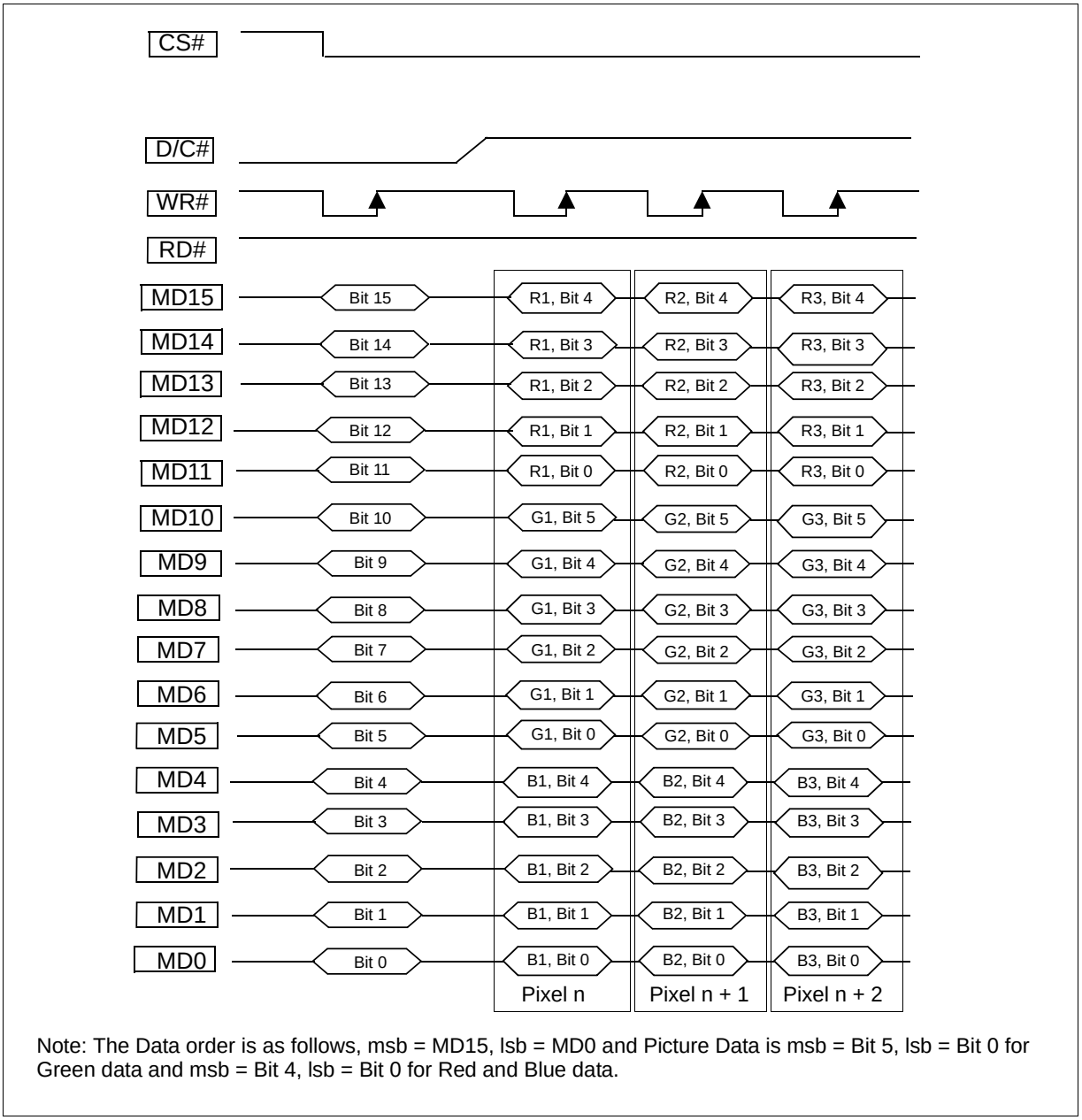


Note: The Data order is as follows, msb = MD15, lsb = MD0 and Picture Data is msb = Bit 2, lsb = Bit 0 for Red and Green data and msb = Bit 1, lsb = Bit 0 for Blue data.

Figure 13-1: 8 bpp (RGB 3:3:2), 256 colors

13.2 16 bpp (RGB 5:6:5), 65,536 colors

When REG[60h] bits 3-0 = 0001b and CNF[1:0] = 11, the input data format for the Intel 80 Host interface is RGB 5:6:5.

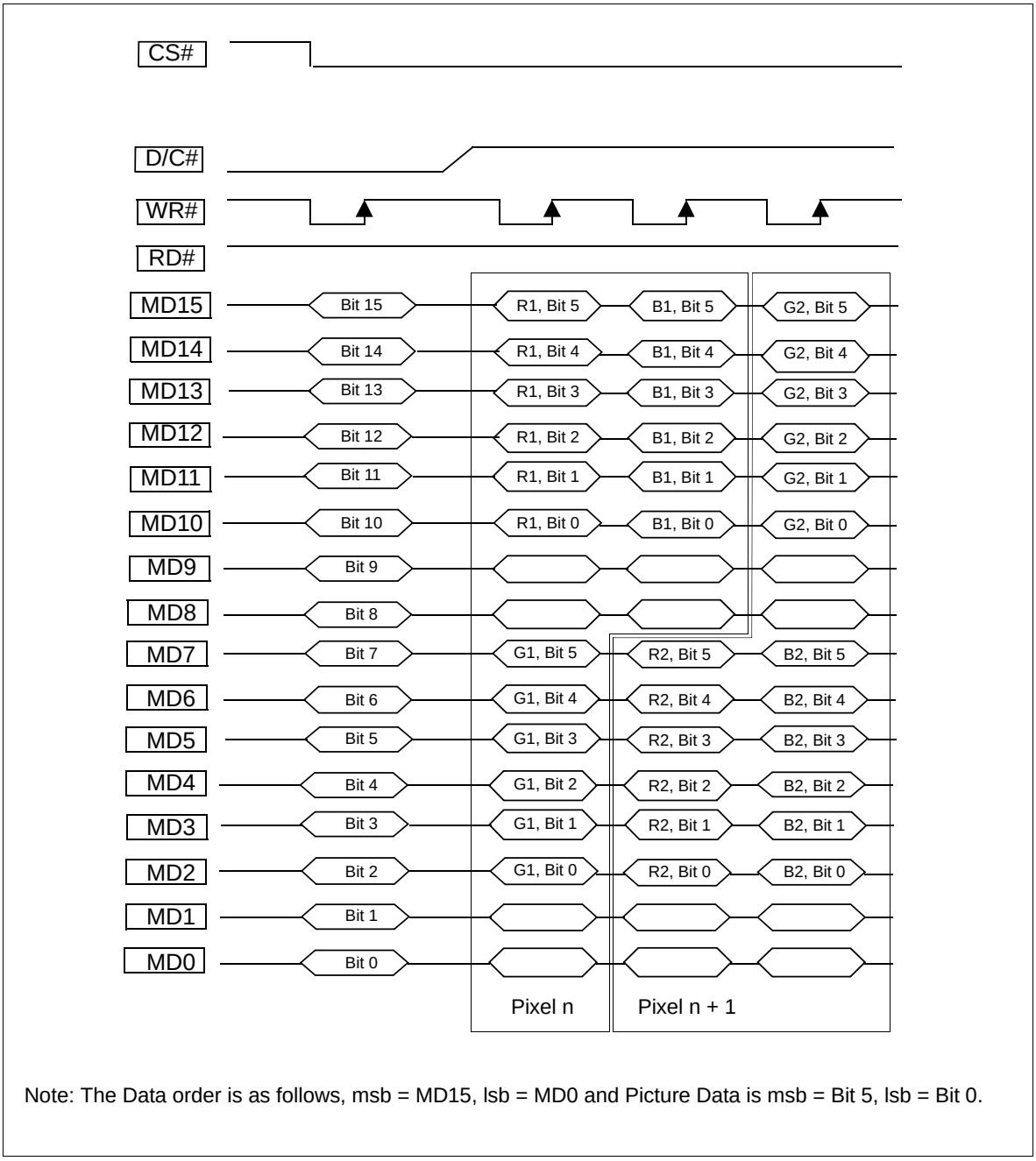


Note: The Data order is as follows, msb = MD15, lsb = MD0 and Picture Data is msb = Bit 5, lsb = Bit 0 for Green data and msb = Bit 4, lsb = Bit 0 for Red and Blue data.

Figure 13-2: 16 bpp (RGB 5:6:5), 65,536 colors

13.3 18 bpp Mode 1 (RGB 6:6:6), 262,144 colors

When REG[60h] bits 3-0 = 0010b and CNF[1:0] = 11, the input data format for the Intel 80 Host interface is RGB 6:6:6 mode 1.

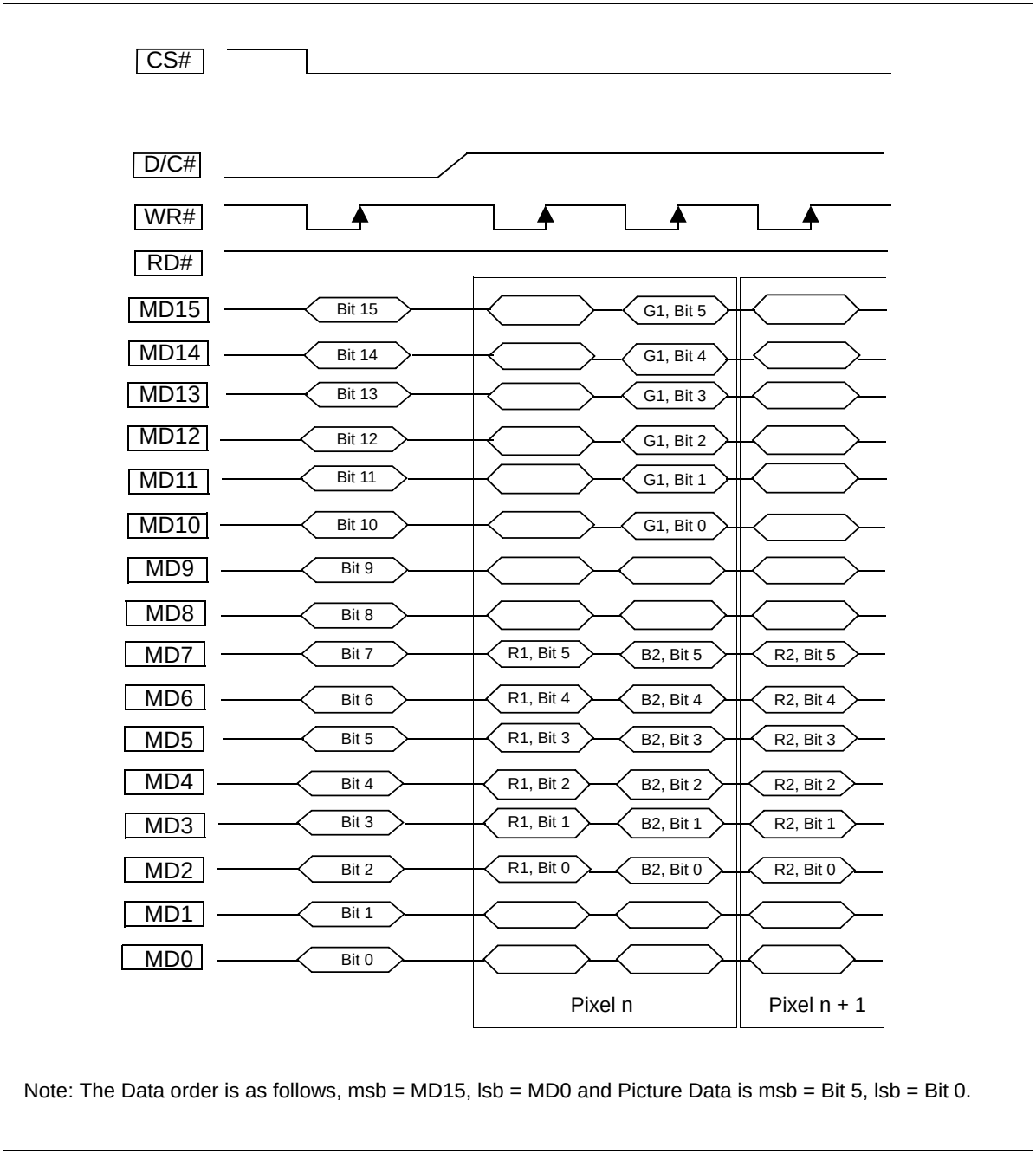


Note: The Data order is as follows, msb = MD15, lsb = MD0 and Picture Data is msb = Bit 5, lsb = Bit 0.

Figure 13-3: 18 bpp Mode 1 (RGB 6:6:6), 262,144 colors

13.4 18 bpp Mode 2 (RGB 6:6:6), 262,144 colors

When REG[60h] bits 3-0 = 0110b and CNF[1:0] = 11, the input data format for the Intel 80 Host interface is RGB 6:6:6 mode 2.

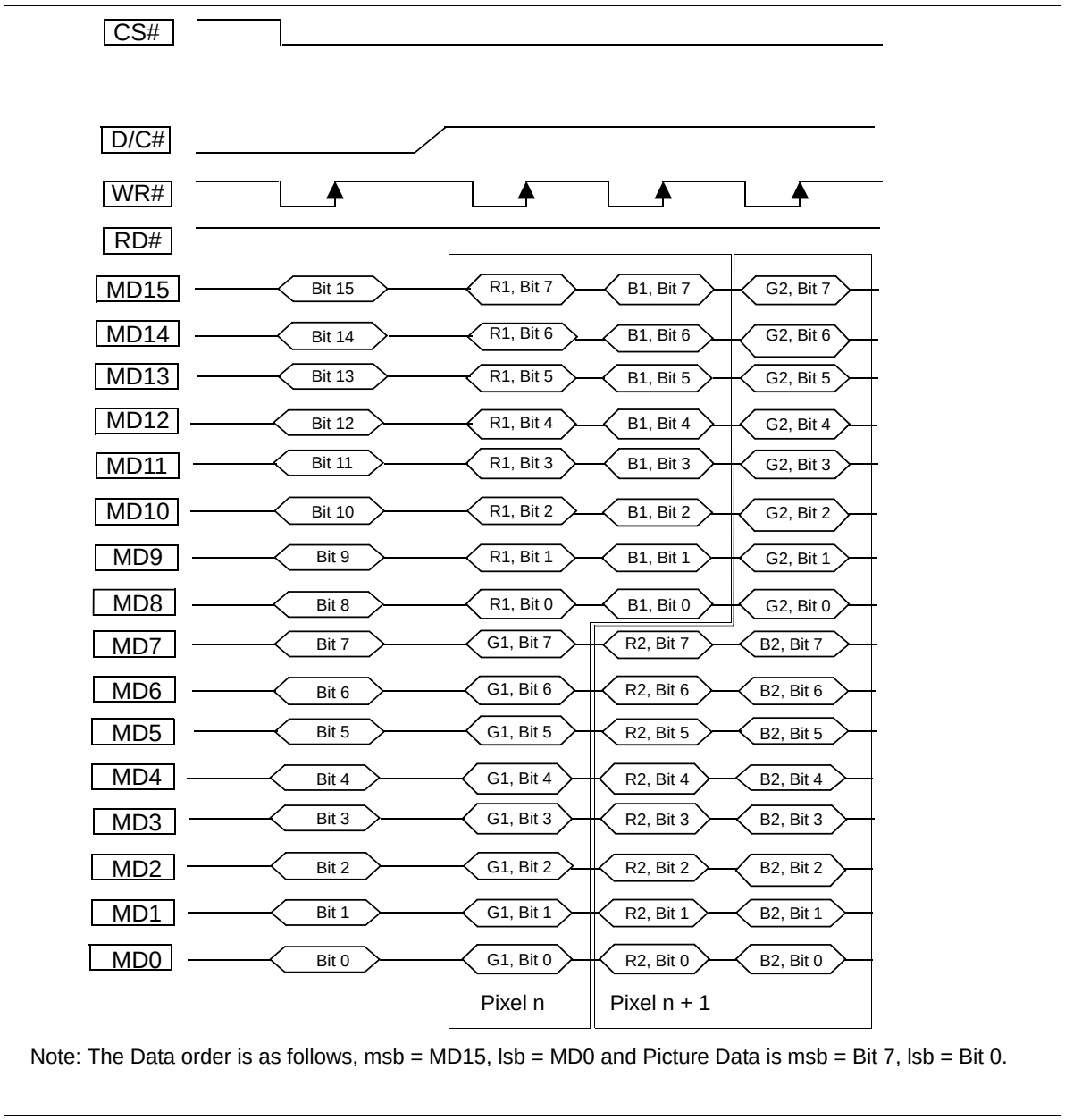


Note: The Data order is as follows, msb = MD15, lsb = MD0 and Picture Data is msb = Bit 5, lsb = Bit 0.

Figure 13-4: 18 bpp Mode 2 (RGB 6:6:6), 262,144 colors

13.5 24 bpp Mode 1 (RGB 8:8:8), 16,777,216 colors

When REG[60h] bits 3-0 = 0011b and CNF[1:0] = 11, the input data format for the Intel 80 Host interface is RGB 8:8:8 mode 1.

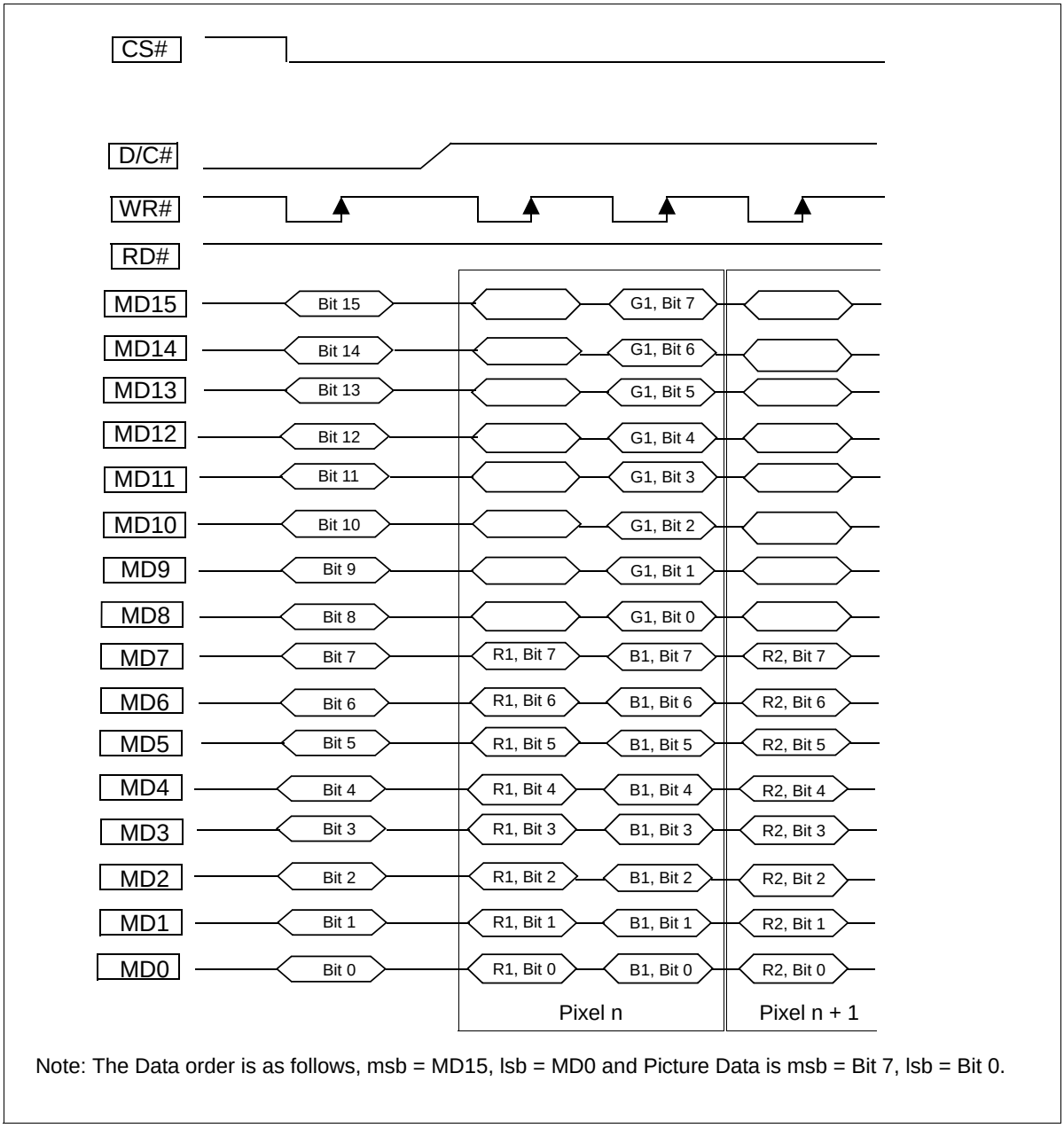


Note: The Data order is as follows, msb = MD15, lsb = MD0 and Picture Data is msb = Bit 7, lsb = Bit 0.

Figure 13-5: 24 bpp Mode 1 (RGB 8:8:8), 16,777,216 colors

13.6 24 bpp Mode 2 (RGB 8:8:8), 16,777,216 colors

When REG[60h] bits 3-0 = 0111b and CNF[1:0] = 11, the input data format for the Intel 80 Host interface is RGB 8:8:8 mode 2.



Note: The Data order is as follows, msb = MD15, lsb = MD0 and Picture Data is msb = Bit 7, lsb = Bit 0.

Figure 13-6: 24 bpp Mode 2 (RGB 8:8:8), 16,777,216 colors

14 YUV Timing

Format Definition

- The number of pixels per line is always even
- The YC_BC_R colorspace is defined in ITU-R BT601.4
- YUV 4:2:2 format
  $U_{11}Y_{11}V_{11}Y_{12}U_{13}Y_{13}V_{13}Y_{14}$...
- YUV 4:2:0 format
  Odd Line: $UY_{11}Y_{12}$...
  Even Line: $VY_{21}Y_{22}$...

Note
When a window is setup for YUV data, the data must always alternate between odd and even lines, starting with an odd line.

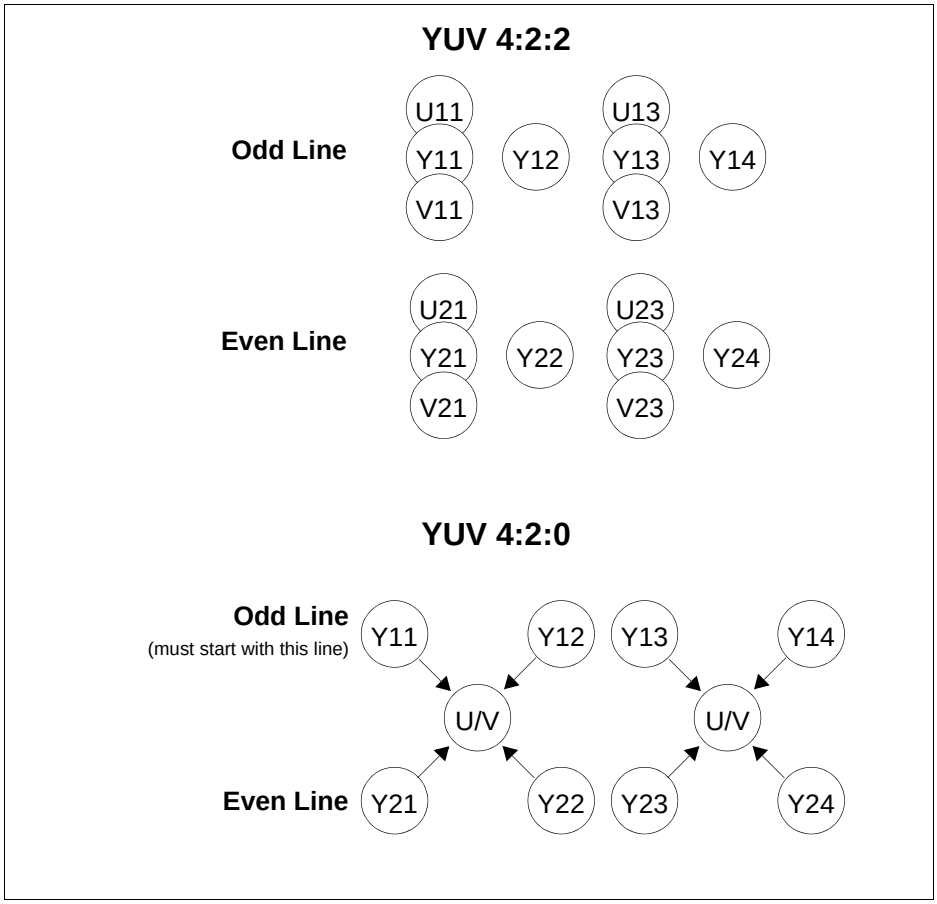


Figure 14-1: YUV Format Definition

14.1 YUV 4:2:2 with Intel 80, 8-bit Interface

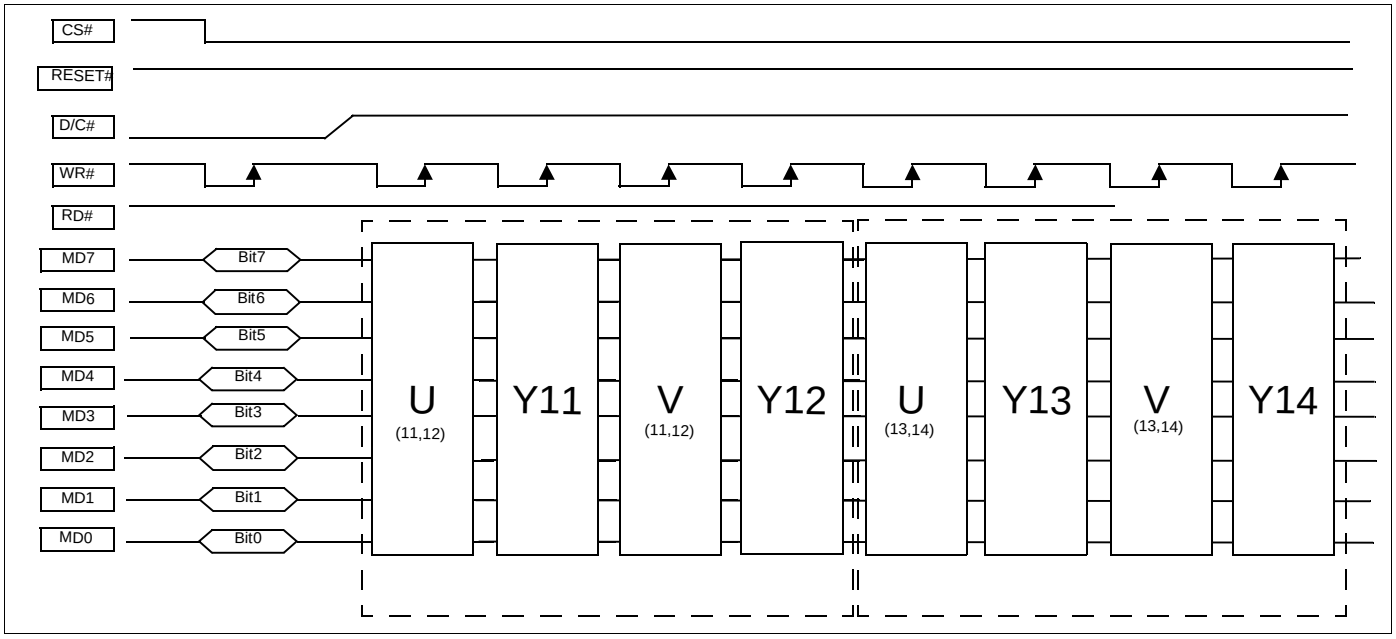


Figure 14-2: YUV 4:2:2 with Intel 80, 8-bit Interface

14.2 YUV 4:2:0 ODD Line with Intel 80, 8-bit Interface

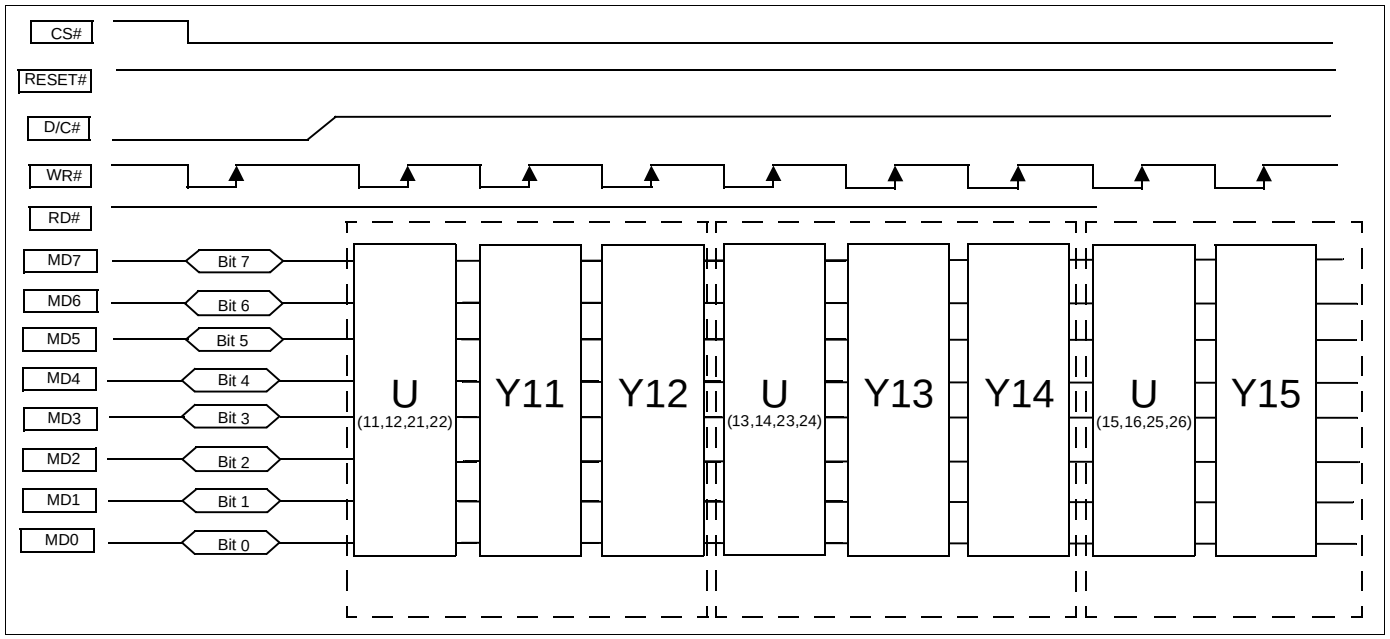


Figure 14-3: YUV 4:2:0 ODD Line with Intel 80, 8-bit Interface

14.3 YUV 4:2:0 EVEN Line with Intel 80, 8-bit Interface

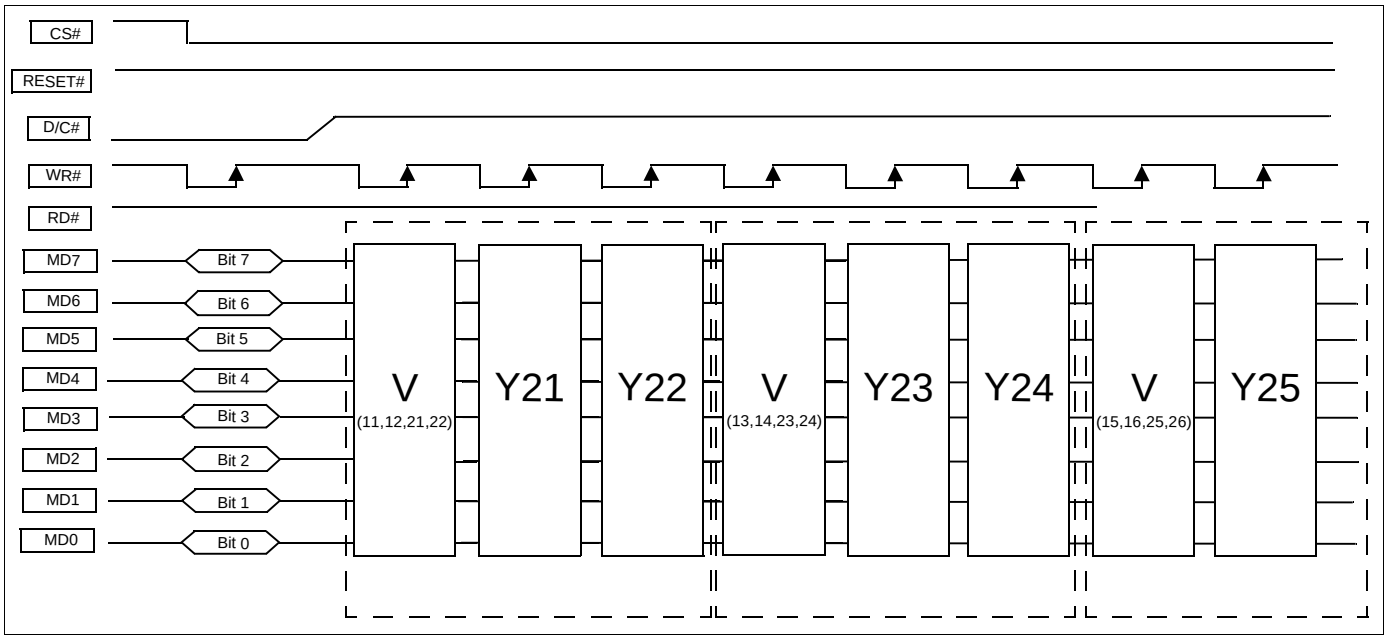


Figure 14-4: YUV 4:2:0 EVEN Line with Intel 80, 8-bit Interface

14.4 YUV 4:2:2 with Intel 80, 16-bit Interface

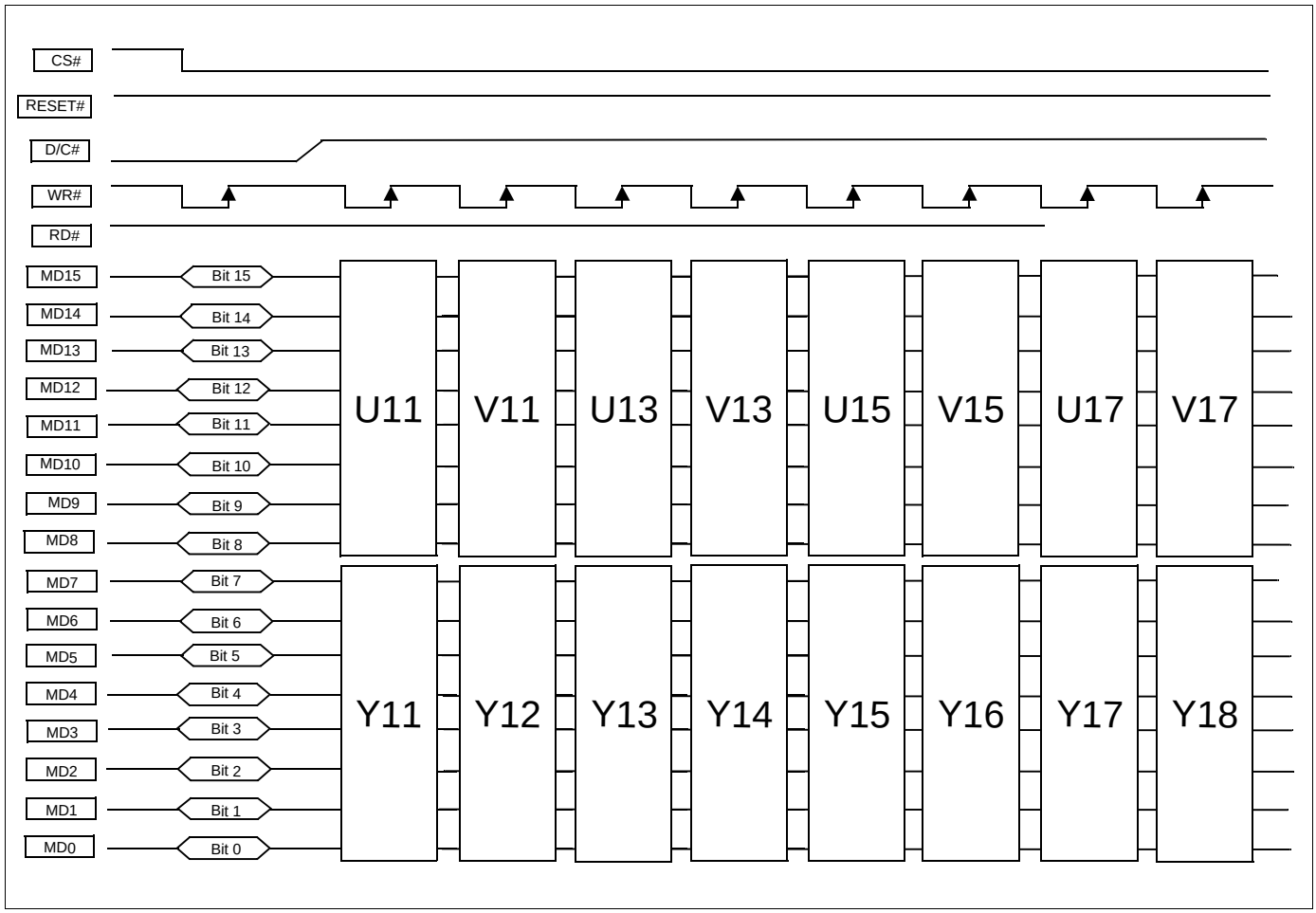


Figure 14-5: YUV 4:2:2 with Intel 80, 16-bit Interface

14.5 YUV 4:2:0 ODD Line with Intel 80, 16-bit Interface

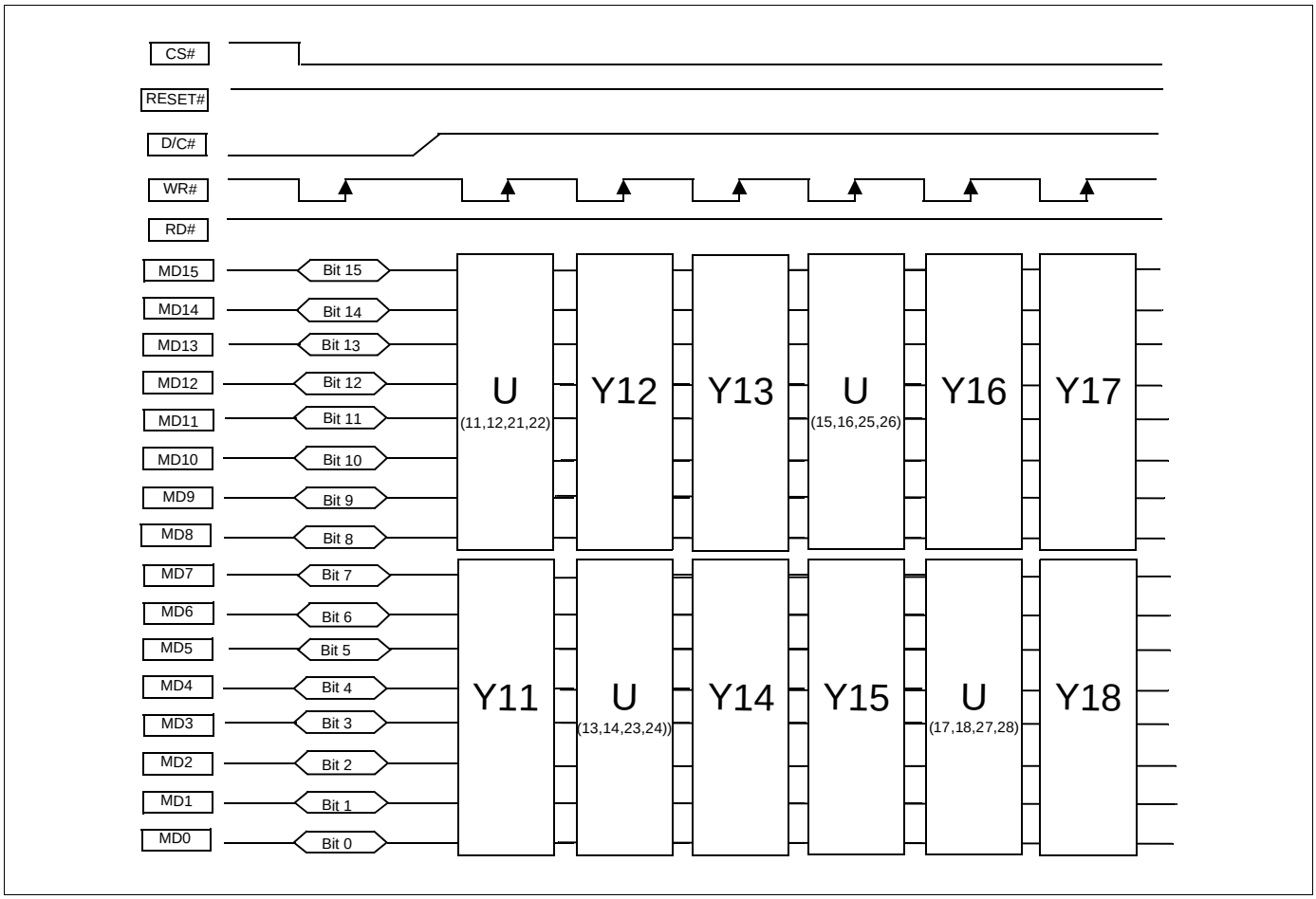


Figure 14-6: YUV 4:2:0 ODD Line with Intel 80, 16-bit Interface

Note

When using this mode, the input window width must be divisible by 4.

14.6 YUV 4:2:0 EVEN Line with Intel 80, 16-bit Interface

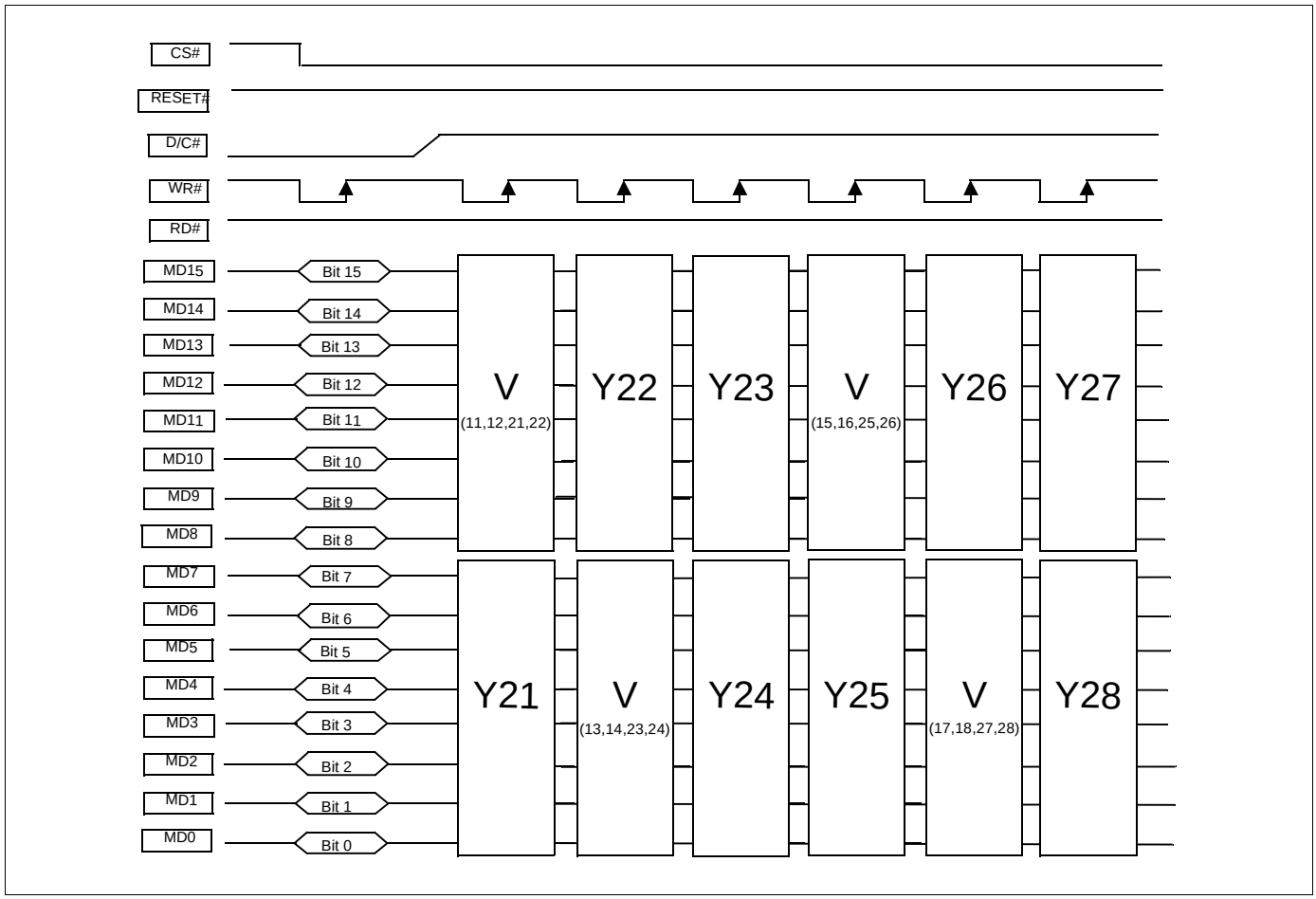


Figure 14-7: YUV 4:2:0 EVEN Line with Intel 80, 16-bit Interface

15 SwivelView™

15.1 SwivelView™ Concept

Most computer displays are refreshed in landscape orientation – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView is designed to rotate the displayed image on a TV by 90 ·, 180 ·, or 270 · in a counter-clockwise direction1 The rotation is done in hardware and is transparent to the user for all display buffer writes. By processing the rotation in hardware, SwivelView offers a performance advantage over software rotation of the displayed image.

The actual address translation is performed during the Host Write and the image data is, therefore, stored in memory in it's rotated orientation. Due to this design of the rotation logic, all windows written to the S1D13746 can be independently rotated with respect to each other.

15.2 90° SwivelView™

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13746 in the following sense: A–B–C–D. The display is refreshed in the following sense: B-D-A-C.

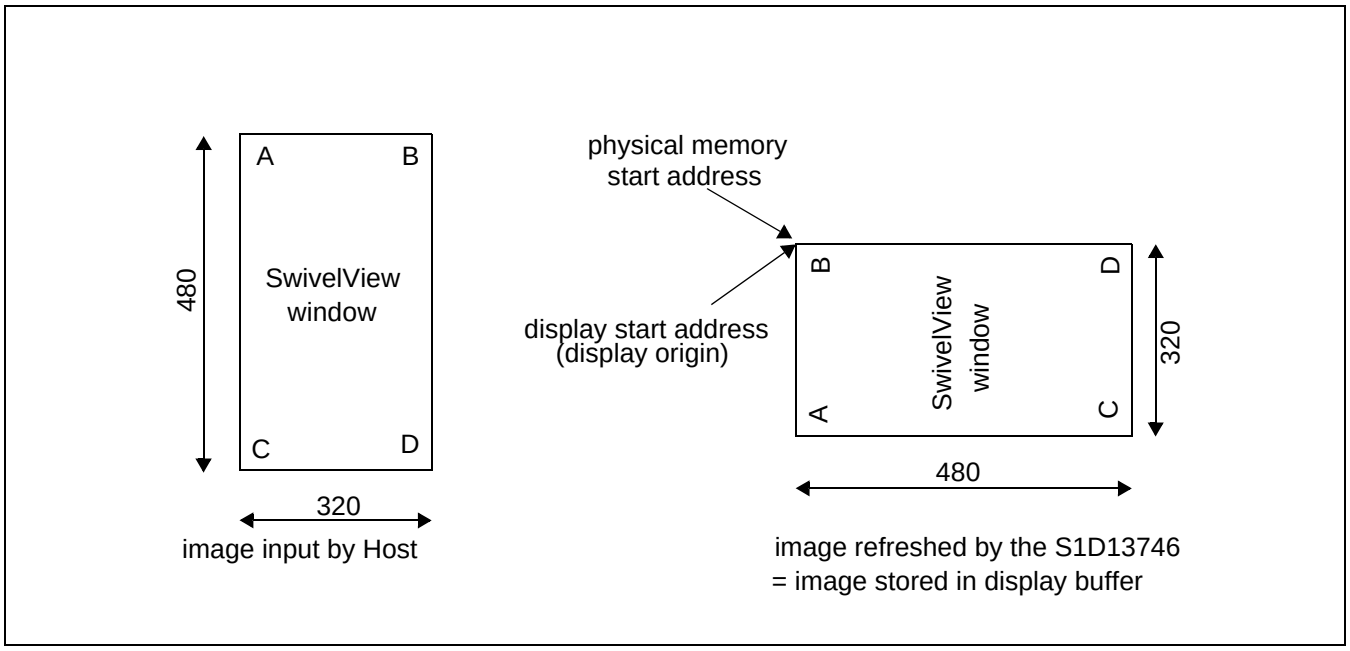


Figure 15-1: Relationship Between the Screen Image and the Image Refreshed in 90° SwivelView

15.2.1 Register Programming

There are no special programming requirements other than enabling the rotation (see REG[62h] bits 1-0). The start address and line offset are automatically calculated by the hardware.

15.3 180° SwivelView™

The following figure shows how the programmer sees a 480x320 landscape image and how the image is being displayed. The application image is written to the S1D13746 in the following sense: A–B–C–D. The display is refreshed in the following sense: D-C-B-A.

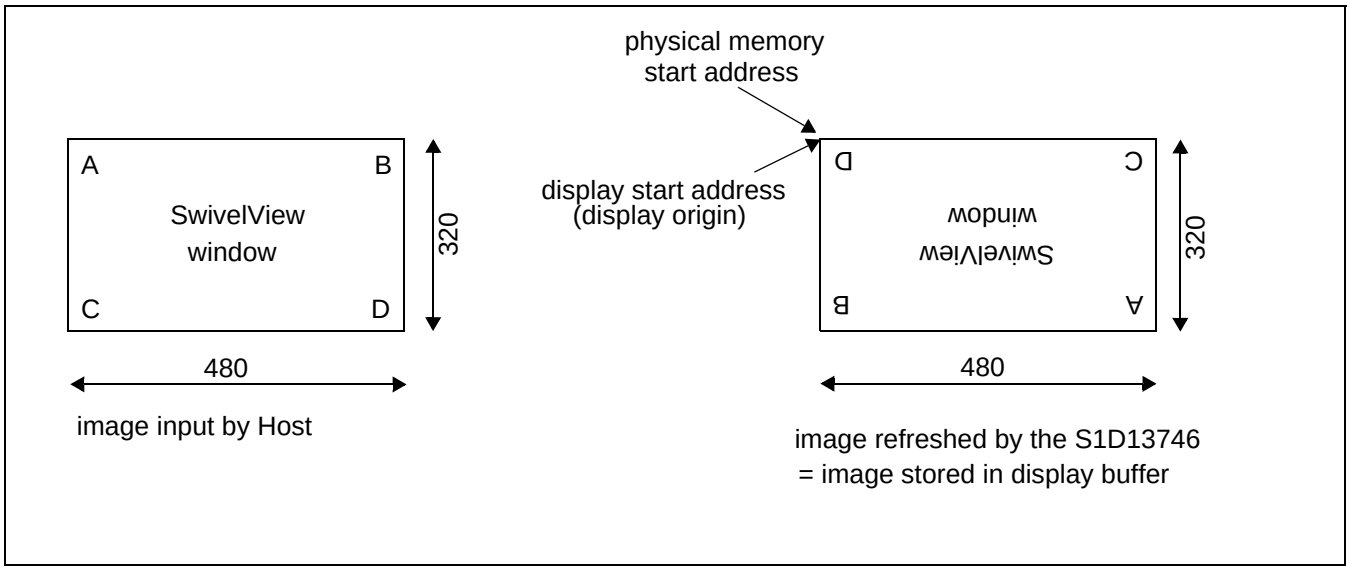


Figure 15-2: Relationship Between the Screen Image and the Image Refreshed in 180° SwivelView

15.3.1 Register Programming

There are no special programming requirements other than enabling the rotation (see REG[62h] bits 1-0). The start address and line offset are automatically calculated by the hardware.

15.4 270° SwivelView™

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13746 in the following sense: A–B–C–D. The display is refreshed in the following sense: C-A-D-B.

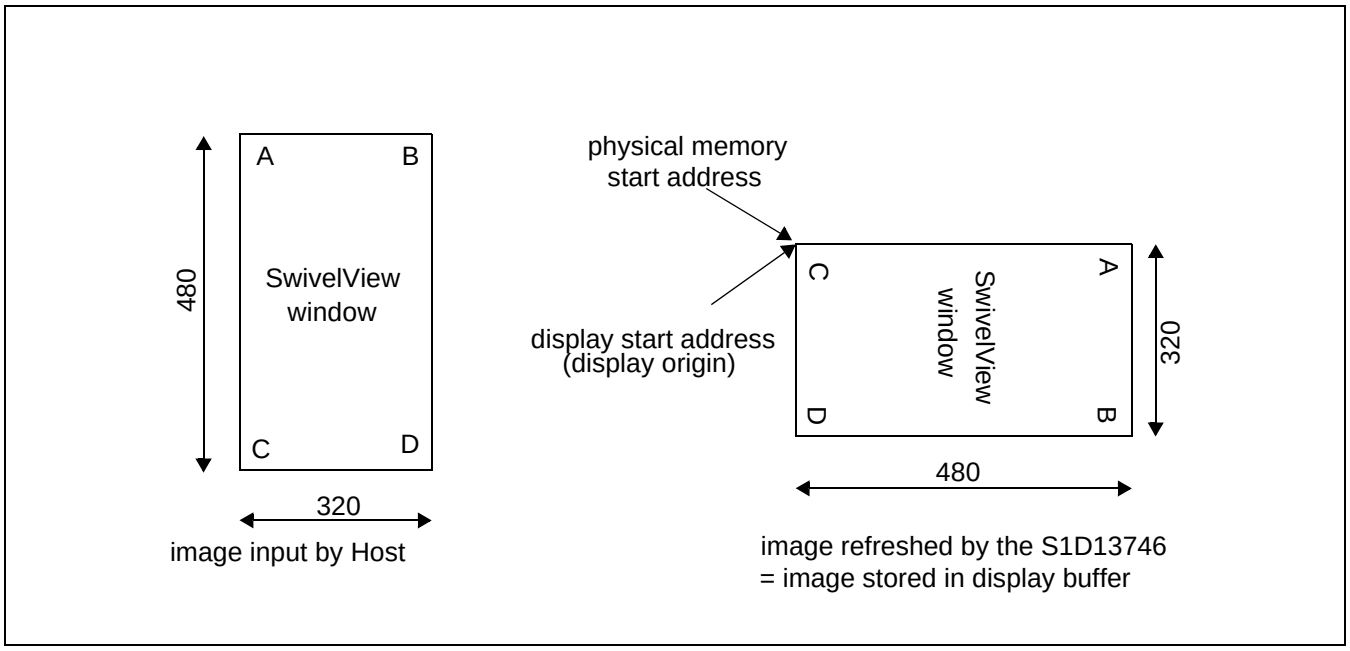


Figure 15-3: Relationship Between the Screen Image and the Image Refreshed in 270° SwivelView

15.4.1 Register Programming

There are no special programming requirements other than enabling the rotation (see REG[62h] bits 1-0). The start address and line offset are automatically calculated by the hardware.

15.5 Sub-Window Position / Rotation

In a typical environment, all windows are rotated in the same orientation. However, it is conceivable that individual windows require independent rotation. The examples below show all Use Cases with emphasis placed on the fact that window position is always based on top-left corner of the main display image and the top-left corner of the new window independent of their rotations.

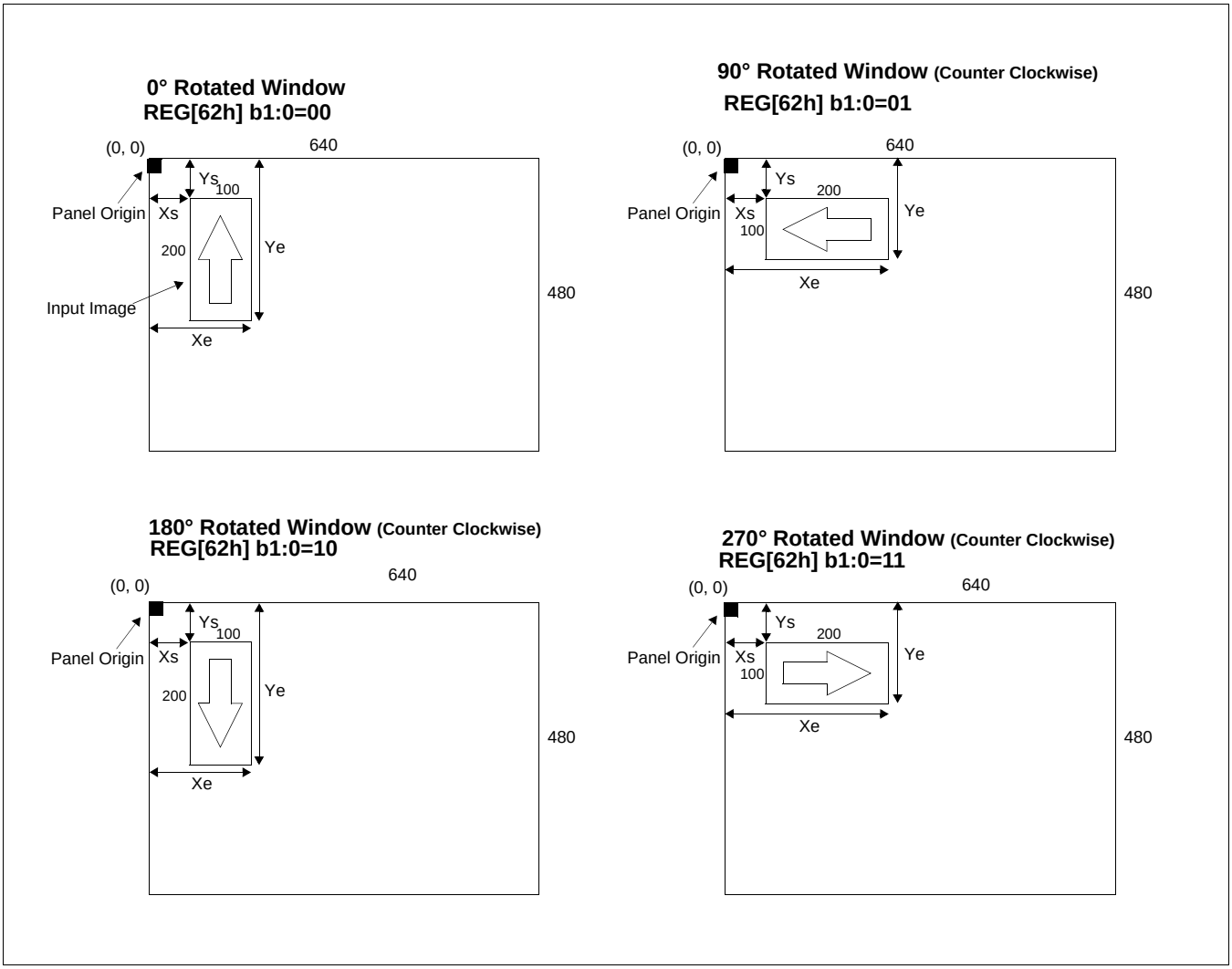


Figure 15-4: Sub-window position / rotation

Where:

All rotations: Xs = REG[82h] ~ REG[84h]
Ys = REG[86h] ~ REG[88h]
0°, 180°: Xe = Xs + Input Window Width (REG[68h] ~ REG[6Ah])
Ye = Xs + Input Window Height (REG[64h] ~ REG[66h])
90°, 270°: Xe = Xs + Input Window Height (REG[64h] ~ REG[66h])
Ye = Xs + Input Window Width (REG[68h] ~ REG[6Ah])

16 Image Enhancement Engine

The Image Enhancement Engine (IEE) provides a 3x3 filter which allows the S1D13746 to manipulate images. When data is sent to the filter for processing, the data path is as follows.

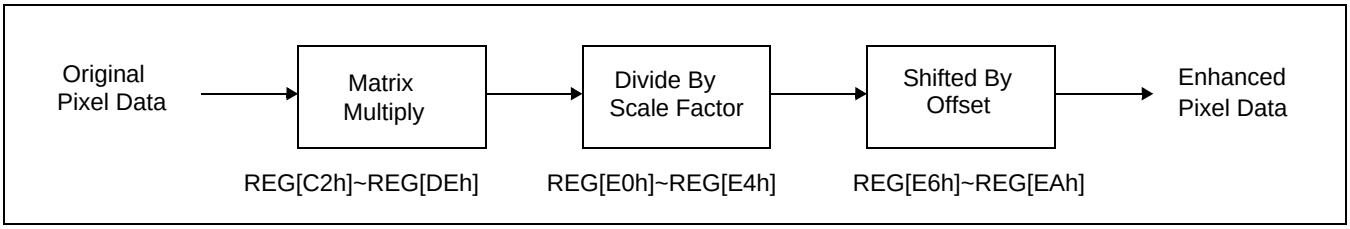


Figure 16-1 Image Enhancement Filter Overview

16.1 3x3 Filter

Note
SYSCLK must be 54MHz when 3x3 filter is enabled

The 3x3 filter function can manipulate each pixel in an image by calculating the intensity of neighboring pixels using a 3x3 matrix. The following figure describes the operation of the 3x3 filter.

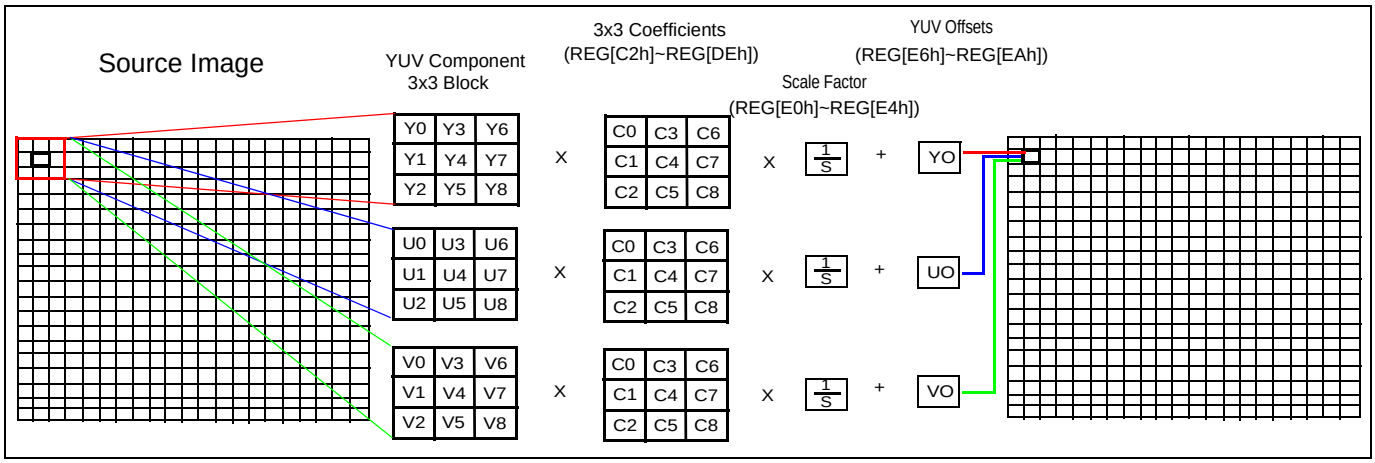


Figure 16-2: 3x3 Filter Matrix Function

The 3x3 filter scans through every pixel in an image and its neighboring pixels. Each YUV component block is calculated based on the programmable 3x3 coefficients (REG[C2h] ~ REG[DEh]), scaling rate (REG[E0h] ~ REG[E4h]), and offsets (REG[E6h] ~ REG[EAh]). The following figure provides some examples of the possible visual effects.

Note
For visual effect example programming values, see Section 16.1.1, “Example Programming Values” on page 142.

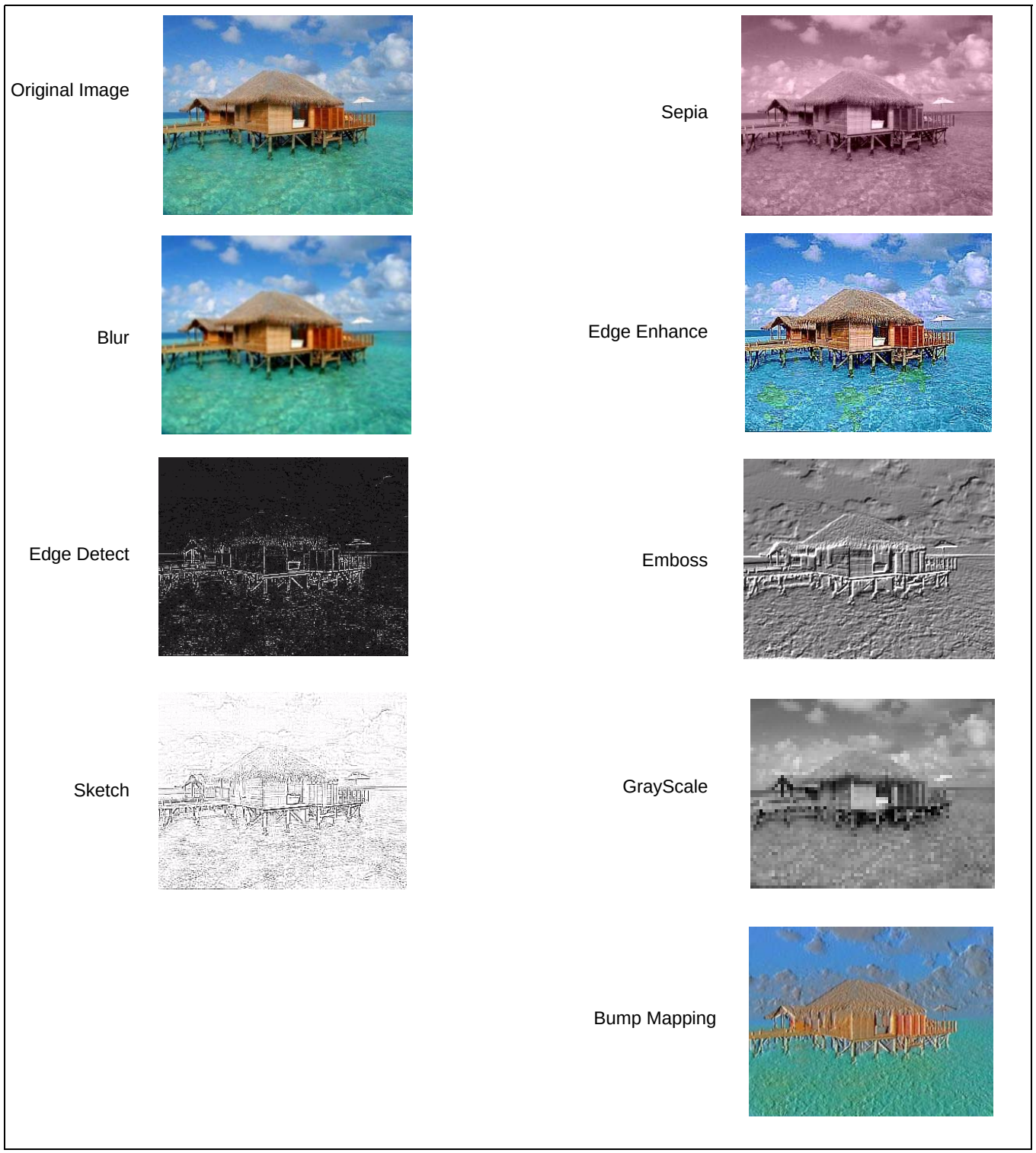


Figure 16-3: Filter Visual Effect Examples

16.1.1 Example Programming Values

The following table provides example values that can be used to achieve various visual effects using the 3x3 filter.

Table 16-1: 3X3 Pixel Matrix Filter Function Programming Values

Register Programming	Filter Functions										
	Bypass (Default)	**Sharp**	**Blur**	**Edge Detect**	**Sketch**	**Sepia**	**Edge Enhance**	**Emboss**	**Bump Mapping**	**Flicker Filter**	**Dot Crawl + Flicker Filter**
Y0 REG[C2h] bits [2:0]	0h	7h	1h	7h	7h	0h	7h	1h	7h	0h	0h
Y1 REG[C2h] bits [6:4]	0h	7h	1h	7h	7h	0h	7h	1h	7h	0h	0h
Y2 REG[C4h] bits [2:0]	0h	7h	1h	7h	7h	0h	7h	0h	7h	0h	0h
Y3 REG[C4h] bits [6:4]	0h	7h	1h	7h	7h	0h	7h	1h	0h	1h	1h
Y4 REG[C6h] bits [4:0]	01h	09h	1h	08h	08h	01h	0Ah	00h	00h	02h	02h
Y5 REG[C8h] bits [2:0]	0h	7h	1h	7h	7h	0h	7h	7h	0h	1h	1h
Y6 REG[C8h] bits [6:4]	0h	7h	1h	7h	7h	0h	7h	0h	1h	0h	0h
Y7 REG[CAh] bits [2:0]	0h	7h	1h	7h	7h	0h	7h	7h	1h	0h	0h
Y8 REG[CAh] bits [6:4]	0h	7h	1h	7h	7h	0h	7h	7h	1h	0h	0h
U0 REG[CCh] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
U1 REG[CCh] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	2h
U2 REG[CEh] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
U3 REG[CEh] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	1h	1h
U4 REG[D0h] bits [4:0]	01h	09h	01h	08h	00h	00h	01h	00h	01h	02h	02h
U5 REG[D2h] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	1h	1h
U6 REG[D2h] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
U7 REG[D4h] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	2h
U8 REG[D4h] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
V0 REG[D6h] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
V1 REG[D6h] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	2h
V2 REG[D8h] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
V3 REG[D8h] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	1h	1h
V4 REG[DAh] bits [4:0]	01h	09h	01h	08h	00h	00h	01h	00h	01h	02h	02h
V5 REG[DCh] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	1h	1h
V6 REG[DCh] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
V7 REG[DEh] bits [2:0]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	2h
V8 REG[DEh] bits [6:4]	0h	7h	1h	7h	0h	0h	0h	0h	0h	0h	0h
YD (REG[E0h])	01h	01h	09h	01h	01h	01h	02h	01h	01h	04h	04h
UD (REG[E2h])	01h	01h	09h	01h	01h	01h	01h	01h	01h	04h	08h
VD (REG[E4h])	01h	01h	09h	01h	01h	01h	01h	01h	01h	04h	08h
YO (REG[E6h])	00h	00h	00h	00h	75h	00h	00h	40h	40h	00h	00h
UO (REG[E8h])	00h	00h	00h	40h	40h	30h	00h	40h	00h	00h	00h
VO (REG[EAh])	00h	00h	00h	40h	40h	49h	00h	40h	00h	00h	00h

17 Host Interface

17.1 Using the Intel 80 Interface

Accessing the S1D13746 through the Intel 80 host interface is a multiple step process. All Registers and Memory are accessed through register space.

Note

1. **All Register accesses are 8-bit only, except for the Display Memory Data Port. If the Host interface is 16-bits wide (CNF[1:0] = 11b), the lsbs (MD[7:0]) are used for all registers except the Display Memory Data Port.**
2. **For the Display Memory Data Port (REG[A0h]), all 16 bits are used when the Host interface is 16-bits wide (CNF[1:0] = 11b) and only the lower 7 bits are used when the Host interface is 8-bits wide (CNF[1:0] = 01b).**

First, perform a single “Address Write” to setup the register address. Next, perform a “Data Read/Write” to specify the data to be stored or read from the registers or memory specified in the “Address Write” cycle. Subsequent data read/writes without an address write to change the register address, will automatically “auto” increment the register address, or the internal memory address if accessing the Display Memory Data Port (REG[A0h]), or TV Filter Coefficient and User Clock Ratio Data register (REG[56h]), or Macrovision Data register (REG[5Ah].

To write display data to a window aperture, specify the window size and coordinates followed by the burst data writes to the Display Memory Data Port required to fill the window. In this sequence, the internal memory addressing is automatic (see examples).

17.1.1 Register Write Procedure

Writing to the S1D13746 registers is a two step process. First the register “index”, or address, must be written. This is followed by the “data” to be placed in the specified register.

1. Perform an address write to setup the register address bits 7-0.
2. Perform a data write to update the register.
3. Additional data writes can be performed as the register addresses will be auto incremented.

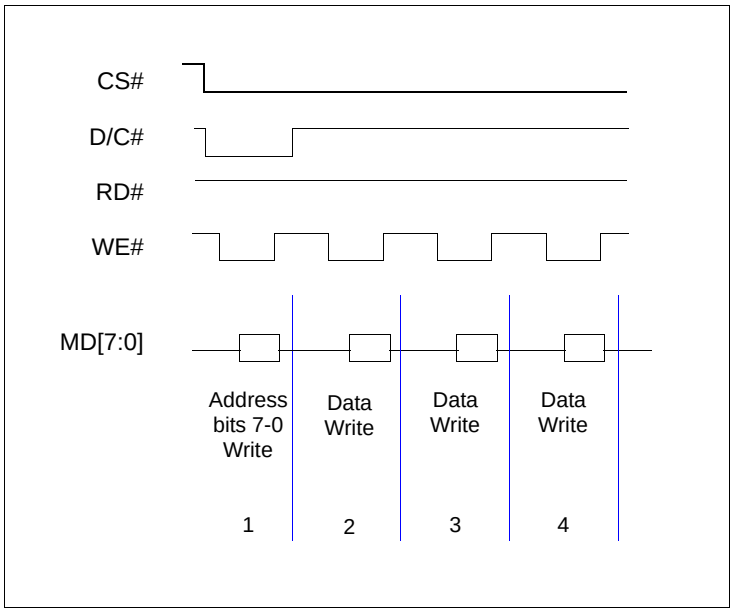


Figure 17-1: Register Write Example Procedure

17.1.2 Register Read Procedure

Reading from the S1D13746 registers is a two step process. First the register "index", or address, must be written. Then the "data" can be read from the specified register.

1. Perform an address write to setup the register address bits 7-0.
2. Perform a data read to get the value of the specified register.
3. Additional data reads can be performed as the register addresses will be auto incremented.

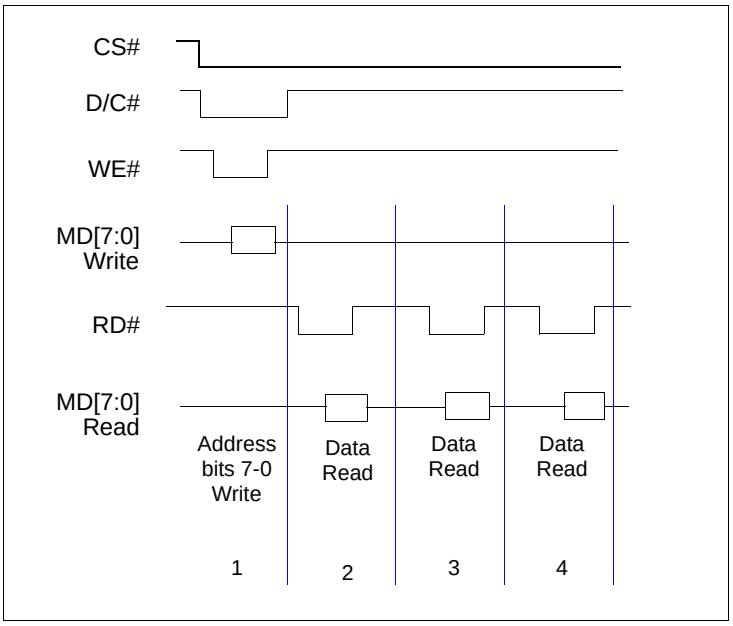


Figure 17-2: Register Read Example Procedure

17.1.3 Sequential Memory Write Procedure

The S1D13746 display memory is written to using the Display Memory Data Port register, REG[A0h]. Once the "index" of the Display Memory Data Port register is written, display data can be burst written to display memory. After each memory write is completed, the internal memory address is automatically incremented.

1. Write to window parameters specified in registers, REG[60h] ~ REG[6Ah] and REG[82h] ~ REG[90h].
2. Perform an address write to setup the Display Memory Data Port address (REG[A0h]).
3. Perform a data write to display memory.
4. The internal memory address is automatically incremented allowing further data writes to display memory.

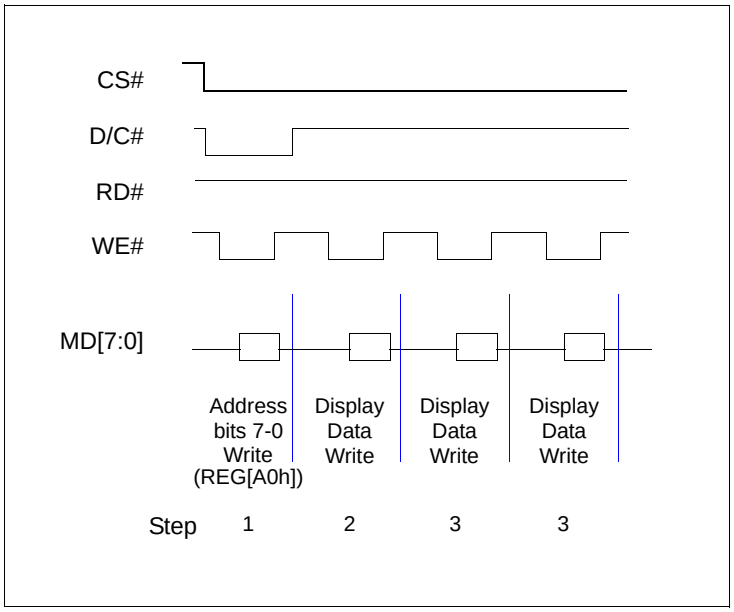


Figure 17-3: Memory Burst Write Example Procedure

Note

Interrupting an image frame write with a register write will reset the frame. After any register write operation, the user must write the entire frame over again.

17.2 Serial Host Interface

The S1D13746 Serial Host Interface supports the following interfaces:

- 3-Wire Serial Interface (9-bit), CNF[1:0] = 00
- 4-Wire Serial Interface (8-bit SPI Interface), CNF[1:0] = 10

17.2.1 3 Wire 9-bit

The 3 wire 9-bit serial interface is selected when CNF[1:0] = 00. The 3 wire 9-bit serial interface consists of a Chip Select (CS#), Serial Clock (SCLK), and a Bi-directional Data pin (SDA). The S1D13746 has a Serial Data Out (SO) pin and a Serial Data In (SI) pin which can be connected together to form the Bi-Directional data pin.

Write and Read Transfers

The following shows the format for a 3-Wire Serial Interface Write Transfer. The first bit of the Command is the D/C# bit which is set to 0b to indicate that it is a Command. The 8 bits, C[7:0] representing the Command, are then sent with the msb first. After the Command, the D/C# bit is set to 1b to indicate that the Data will now be sent. The 8 bits of Data are sent with the msb first. SI is valid on the rising edge of SCLK.

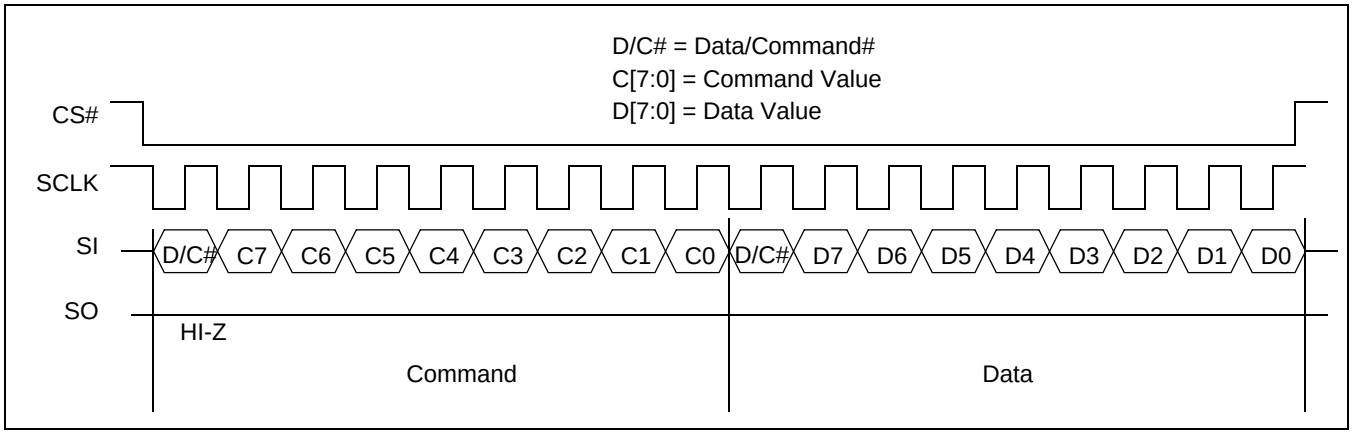


Figure 17-4: Write Transfer

The following figure shows the format for a 3-Wire Serial Interface Read Transfer. The first bit of the Command is the D/C# bit which is set to 0b to indicate that it is a Command. After that the 8 bits C[7:0] representing the Command are sent with the msb first. Then the SI line is deasserted. Now the S1D13746 drives the SO line and sends the 8 bits of data with the msb first. The S1D13746 will drive the line until the CS# goes high. SI is valid at the rising edge of SCLK. SO is launched at the falling edge of SCLK.

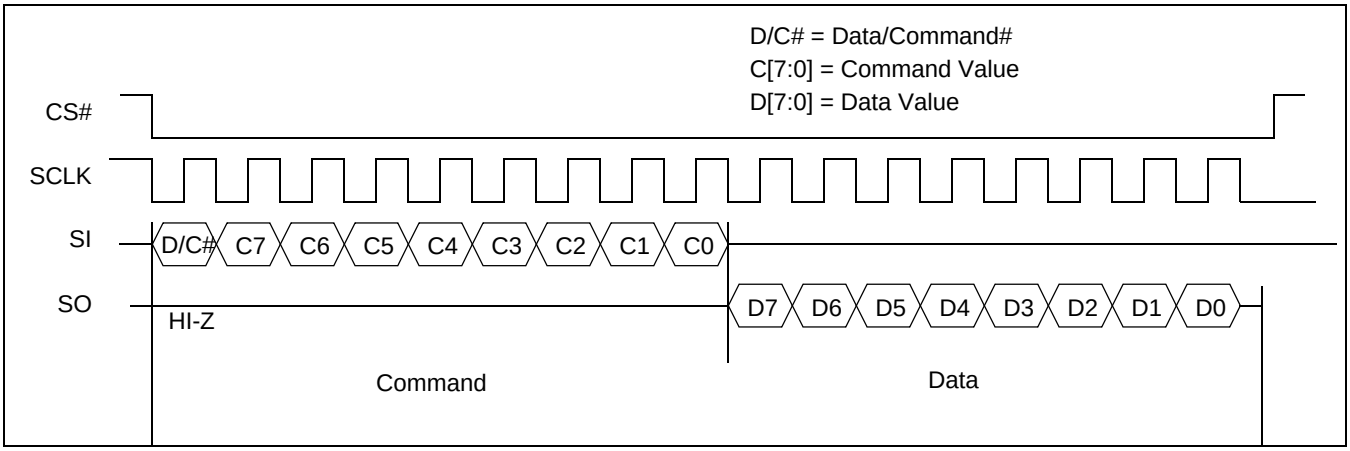


Figure 17-5: Read Transfer

Commands

Using the 3-Wire Serial Interface Read and Write Transfers the user can perform the following functions using the S1D13746:

- Set the Register Address to write to or read from
- Write Data to the Register Address
- Read Data from the Register Address
- Write to consecutive Register addresses.
- Read from consecutive Register addresses.

Table 17-1: Commands

Command	Value	3-Wire Serial Interface Transfer	Description
SET_ADDR	0x40	Write	Set the Register Address to access
WRITE	0x80	Write	Write Data to the Register Address
READ	0xC0	Read	Read Data from the Register Address

In order to access a register in the S1D13746 the SET_ADDR Command must be sent first to set the Register Address to access.

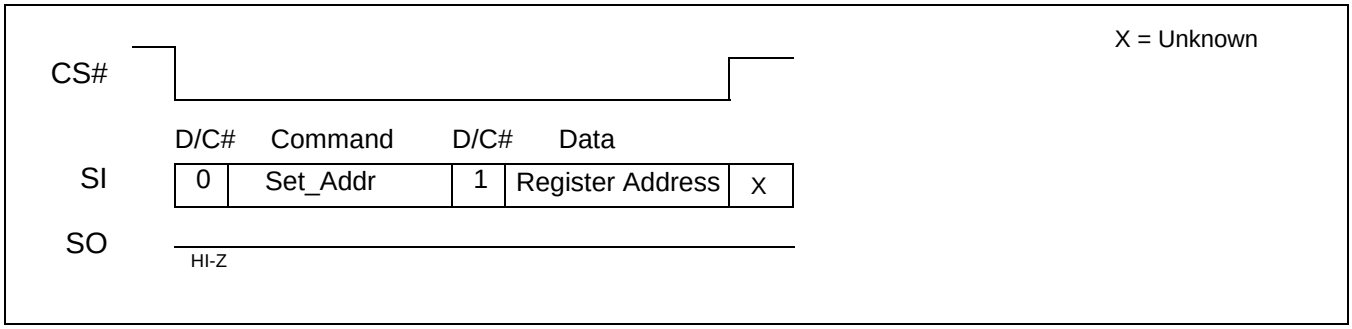


Figure 17-6: Register Address Write

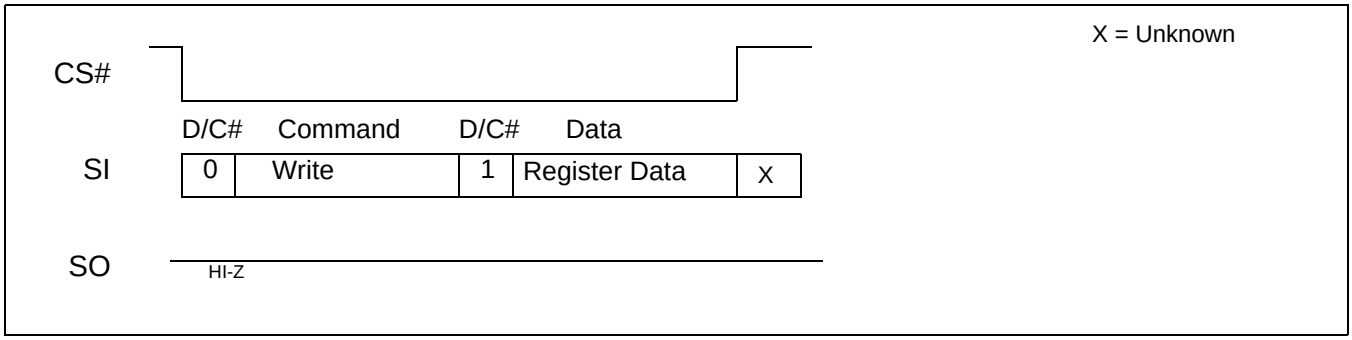


Figure 17-7: Single Register Data Write

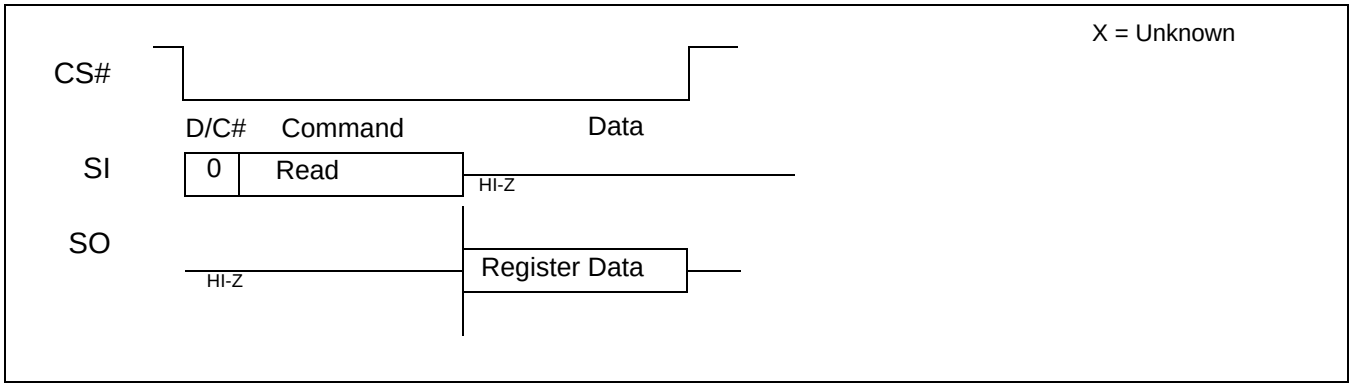


Figure 17-8: Register Data Read

Data can be written to or read from consecutive addresses. After each Data is written or read, the internal Register Address is incremented by 2 to the next address as long as the CS# remains low. For Writes the D/C# bit must precede the Data for each transfer. For Reads the S1D13746 will only send 8 bits of Data for each transfer.

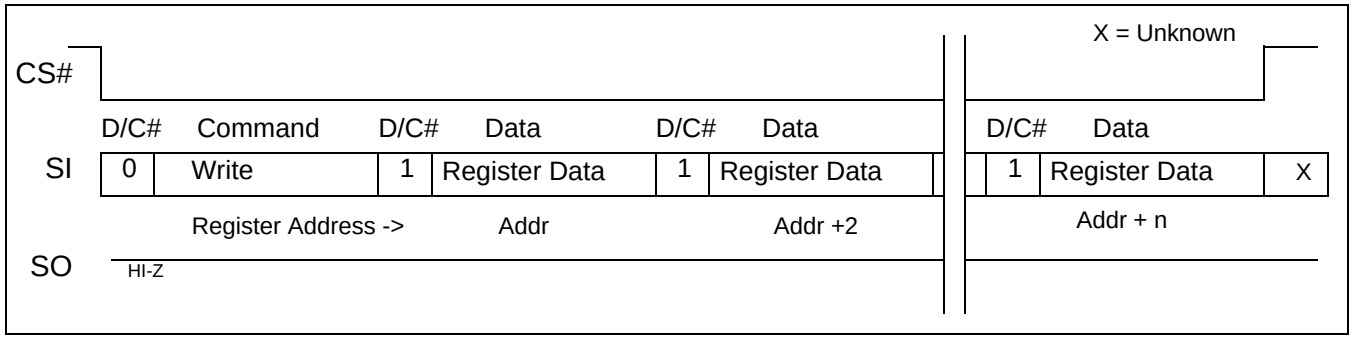


Figure 17-9: Multiple Register Data Writes

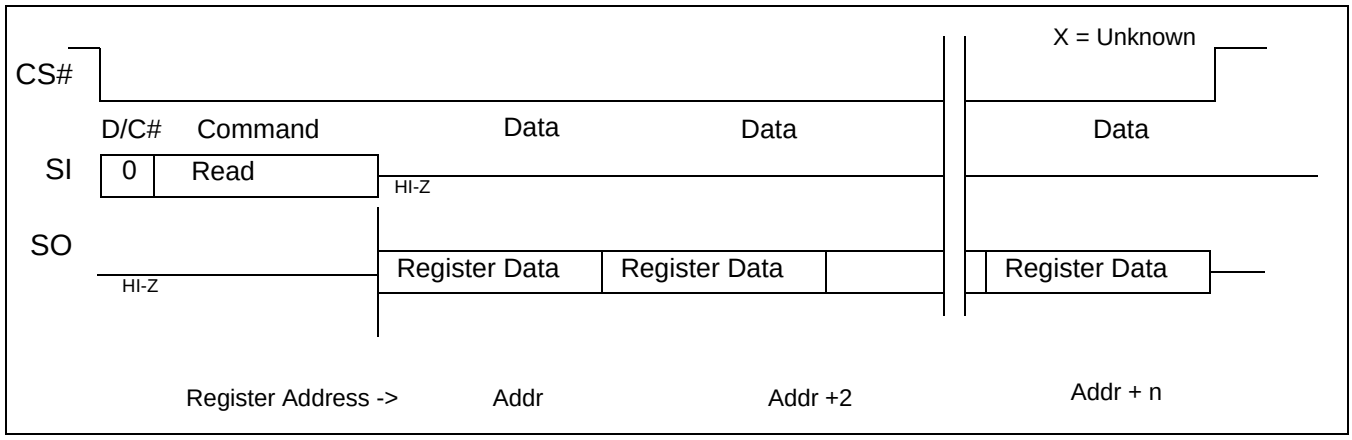


Figure 17-10: Multiple Register Data Reads

17.2.2 SPI Interface

The 4 wire 8-bit serial interface (SPI) is selected when CNF[1:0] = 10b. The SPI interface is comprised of a Chip Select (CS#), Serial Clock (SCLK), Serial Data Out (SO), and a Serial Data In (SI).

SPI Write and Read Transfers

For the SPI Write Transfer the Command C[7:0] is sent after the CS# goes low with the msb first. Following this the Data D[7:0] is sent with the msb first. As long as the CS# is held low then the SO line is driven. SI is valid at the rising edge of SCLK.

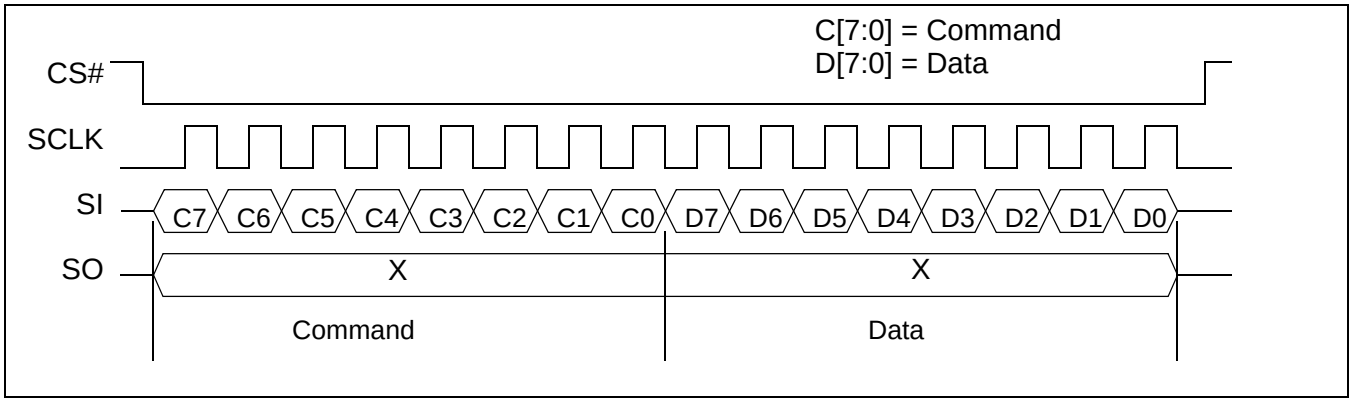


Figure 17-11: SPI Write Transfer

For the SPI Read Transfer the Command C[7:0] is sent after the CS# goes low with the msb first. Following this, the S1D13746 will now send the Data D[7:0] on the SO line with the msb first. During this phase any value on the SI line is ignored. As long as the CS# is held low then the SO line is driven. SI is valid at the rising edge of SCLK. SO is launched at the falling edge of SCLK.

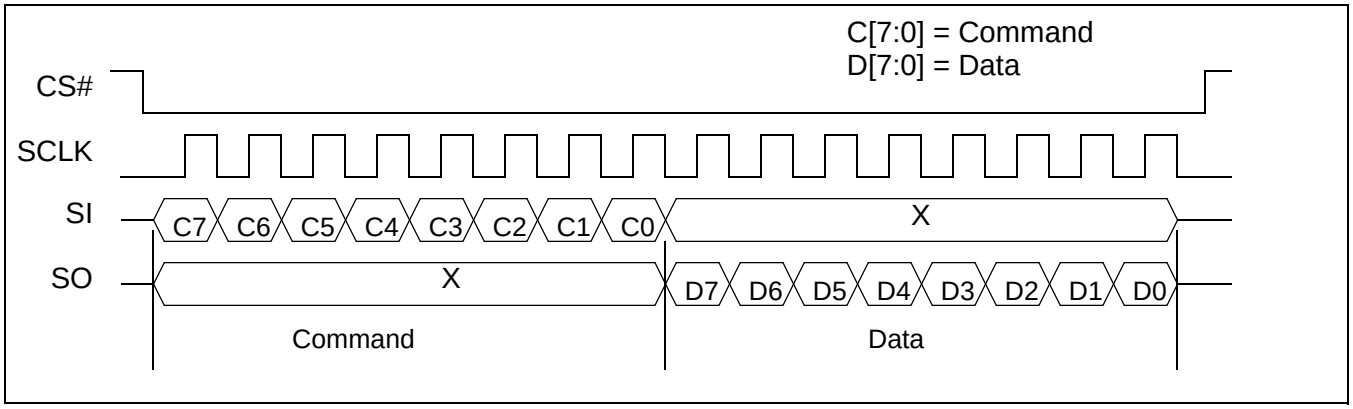


Figure 17-12: SPI Read Transfer

SPI Commands

Using the SPI Read and Write Transfers the user can perform the following functions using the S1D13746:

- Set the Register Address to write to or read from
- Write Data to the Register Address
- Read Data from the Register Address
- Write to consecutive Register addresses.
- Read from consecutive Register addresses.

Table 17-2: SPI Commands

Command	Value	Description
SET_ADDR	0x40	Set the Register Address to Write to
WRITE	0x80	Write Data to the Register Address
READ	0xC0	Read Data from the Register Address

In order to access a register in the S1D13746 the SET_ADDR Command must be sent first to set the Register Address to access.

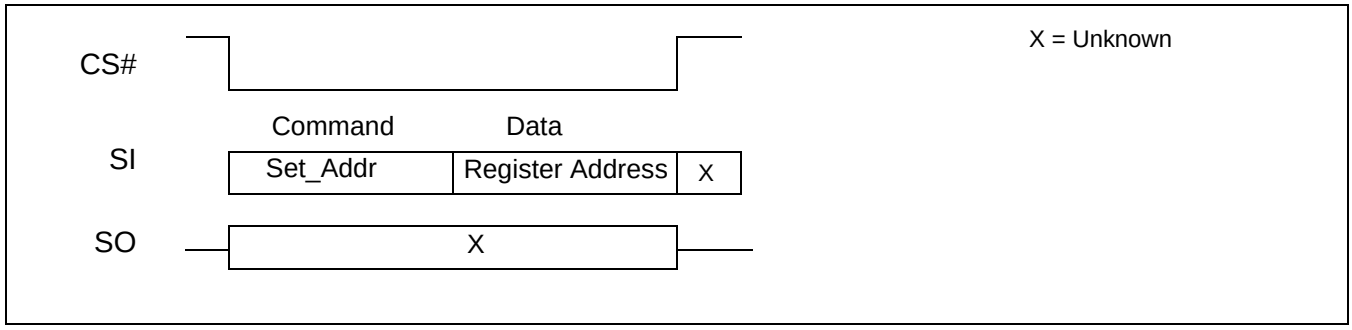


Figure 17-13: Register Address Write

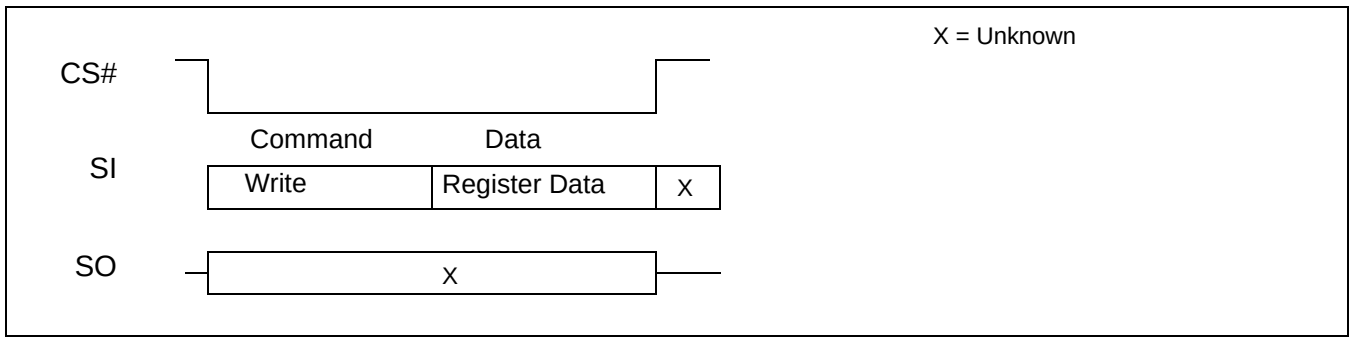


Figure 17-14: Single Register Data Write

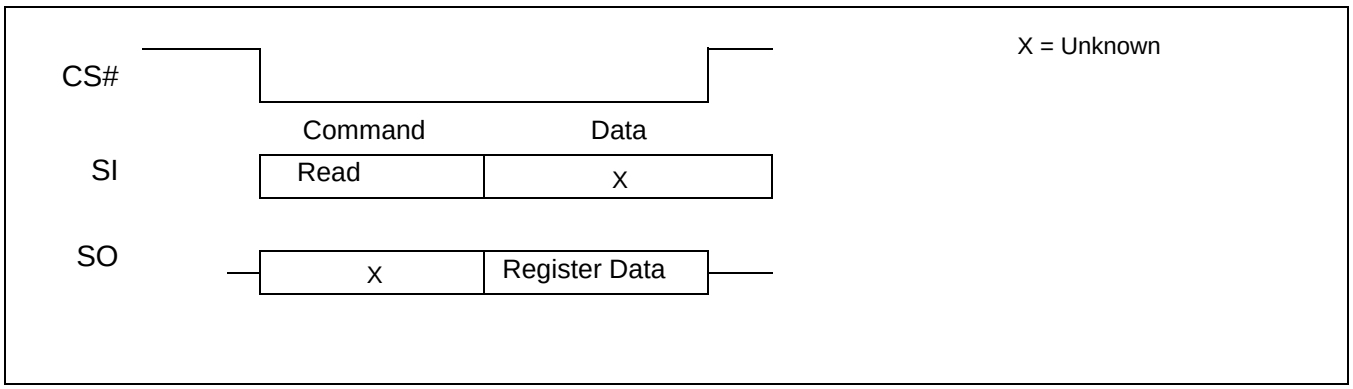


Figure 17-15: Single Register Data Read

Data can be written to or read from consecutive addresses. After each Data is written or read, the internal Register Address is incremented by 2 to the next address as long as the CS# remains low.

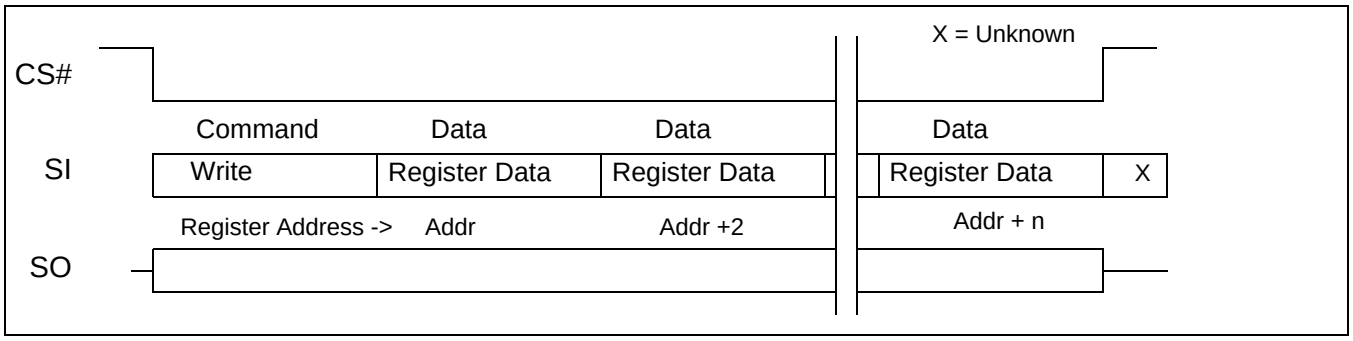


Figure 17-16: Multiple Register Data Writes

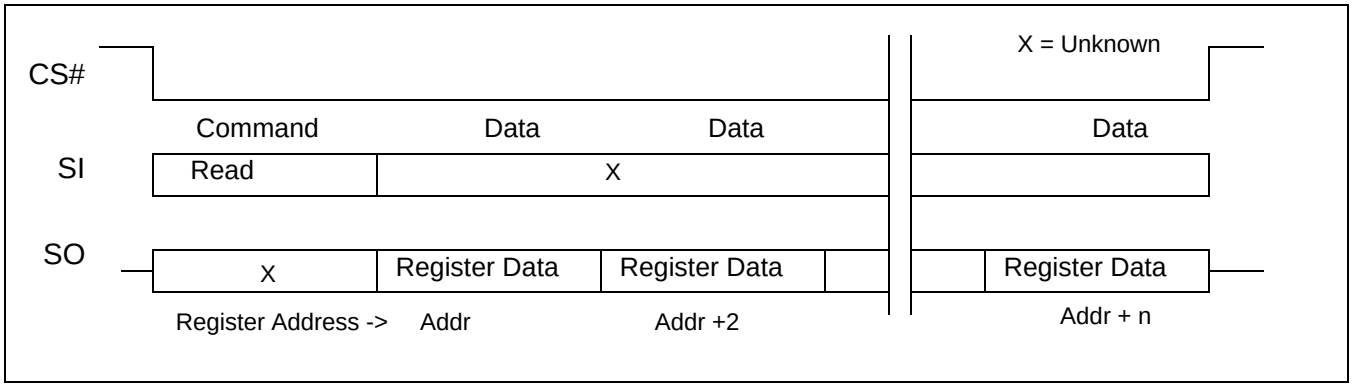


Figure 17-17: Multiple Register Data Reads

18 Parallel RGB Interface Input

When the Parallel RGB Interface input is enabled using the CNF setting, the Host Input Size registers are automatically determined from the Parallel RGB Interface timing. The Display Output Size registers are programmed using a serial interface.

In a typical Parallel RGB Interface implementation, the Input Scaler and Display Output Scaler are only set once after power-up. Since the Host Input Size is always the same (same as the Parallel RGB display resolution), these settings should suffice for all further operation.

The RGB Parallel Interface accepts 18-bit RGB Data along with a Horizontal Sync, Vertical Sync, and a Data Enable signal. The RGB data is fed directly to the TV.

Note

When the Parallel RGB interface is selected, the following restrictions must be met or the Double-Buffer should not be used.

- The input frame rate must be smaller than half of the output (display frame rate).
- The input data burst must be shorter than the output frame period.

18.1 Width and Height Auto Detect

The RGB Parallel Interface can Auto Detect the Width and Height of the input image. By default the Auto Detect is enabled. If the RGB Parallel Interface detects 10 frames of the same height then it will set the Input Size registers with the width and height and will output the 11th frame and every frame thereafter to the TV.

If the Host writes to any of the Input Size registers, Auto Detect is disabled and any image data written after is immediately sent to the TV.

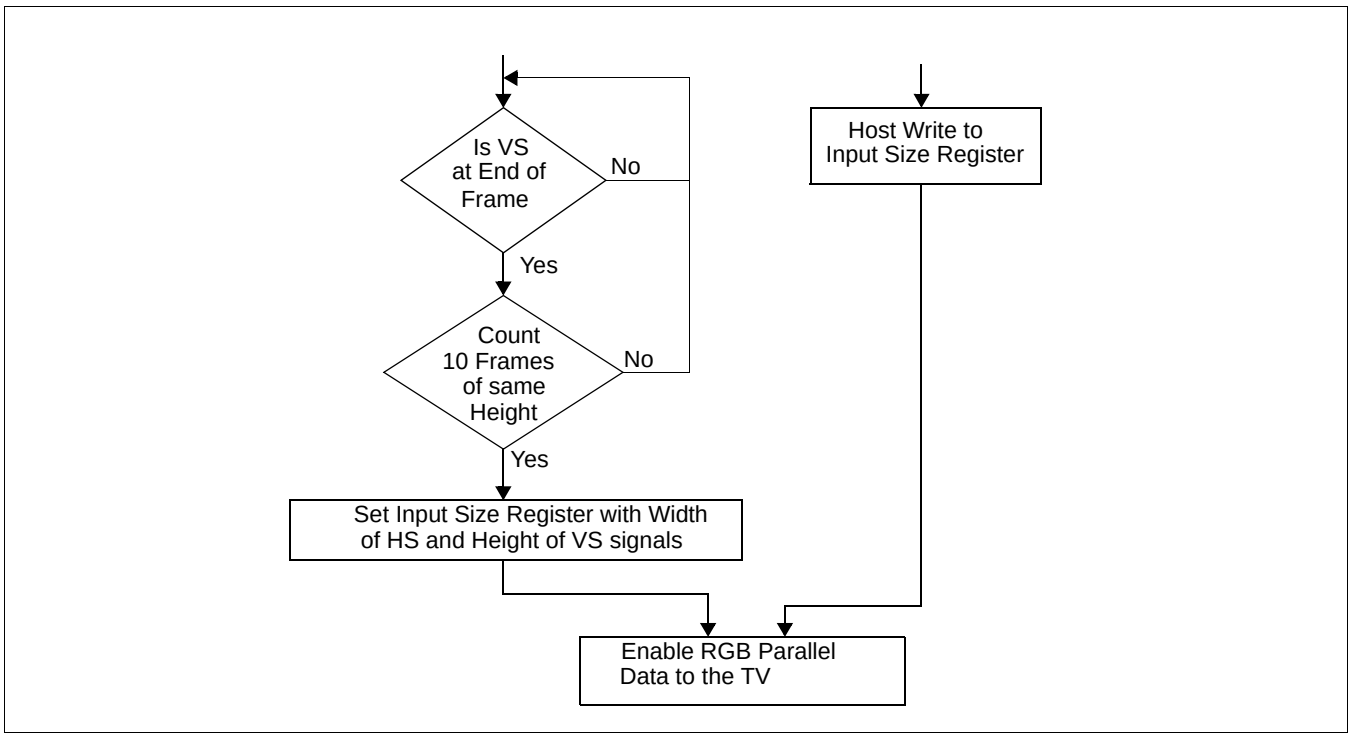


Figure 18-1: Width and Height Auto Detect Flow

19 VBI and Wide-Screen Signalling Function

The S1D13746 supports four VBI/WSS standards:

- ETSI EN 300 294
- ITU-R BT1119-2
- IEC 61880
- CEA-608-B

The above standards specify a method of sending digital information to a TV receiver capable of decoding such data during the Vertical Blanking Interval (VBI) period of the TV output.

The particular line number which the VBI signalling is inserted into depends on the TV output standard. Refer to Table 19-1: “VBI Position” for more information.

The line sequence is referenced to the ITU-R BT.470-6 for 625-line systems (PAL-B/D/G/H/I/N/Nc) and SMPTE for 525-line systems (PAL and NTSC-M).

Table 19-1: VBI Position

			TV Standard			Comments
			NTSC (525 Lines)	**PAL-M (525 Lines)**	**PAL - others (625 Lines)**	
VBI Standard	**ETSI EN 300 294 V1.4.1**	**Line pos**	—	—	23	WSS only. Specified for 625 Line System only Similar to BT.1119-2
		Bits	—	—	14	
		Coding	—	—	Bi-phase	
	ITU-R BT.1119-2 (Implemented in April 2004)	**Line Pos**	22 and 285	22 and 285	23	WSS only For PAL-M, not specified (behaves as 525 Lines system: NTSC)
		Bits	24	24	14	
		Coding	NRZ+ SC Modulate	NRZ+ SC Modulate	Bi-phase	
	CEI 61880	**Line Pos**	20 and 283	—	—	WSS+CMGS+APSFor PAL, not specified
		Bits	20	—	—	
		Coding	NRZ	—	—	
	CEA-608-B	**Line Pos**	21/284	—	22/335	Closed Caption & Extended Data Service (WSS+CMGS+APS) For PAL, not specified For PAL-M, not specified
		Bits	14x2 (2x7x2)	—	14x2 (2x7x2)	
		Coding	NRZ	—	NRZ	

For the ETSI EN 300 294, ITU-R BT1119-2, and IEC 61880, the VBI data is sent out on the above specified line. The VBI data is programmed in REG[42h] ~ REG[48h] and the register bit mapping is specified in the register description.

For CEA-608-B, the standard defines a protocol for sending VBI data, there are two modes of operation as specified in REG[4Ah] bit 1.

- Auto WSS + CGMS + APS
- Manual mode

19.1 CEA-608-B Auto Mode

In Auto Mode, the data programmed into registers REG[42h] ~ REG[48h] is sent out repeatedly as conforming to the protocol outlined in the standard on field 2 (line 284 or 385). In this mode, only information as listed in the register bit mapping of the registers REG[42h] ~ REG[48h] is supported.

The CEA-608-B data is sent out as 16-bit binary sequence (lsb first) on field 2 of the specified VBI line for 8 consecutive TV frames (16 fields). During the CEA-608-B data transmission, field 1 of the specified line contains zero data. During the CEA-608-B data transmission, field 2 contains formatted data as outlined in Table 19-2: “CEA-608-B Auto WSS + CGMS + APS Data Format,” on page 157.

Note
The CEA-608-B data on Field 1 (line 21/22) for CEA-608-B Auto Mode will always contain zero data dummy packet.

The refresh rate of VBI data is determined by REG[48h] bits 2-0 as defined in the register description.

Table 19-2: CEA-608-B Auto WSS + CGMS + APS Data Format

	Bit									Bit								Character	
	0	1	2	3	4	5	6	Parity		0	1	2	3	4	5	6	Parity	Byte 0	Byte 1
XDS Start Current Program: Aspect Ratio Information	1b	0b	0b	0b	0b	0b	0b	0b		1b	0b	0b	1b	0b	0b	0b	1b	01h	89h
Aspect Ratio Information Start/End Line	S0	S1	S2	S3	S4	S5	1b	xb		E0	E1	E2	E3	E4	E5	1b	xb	REG[42h] bits [5:0]	REG[44h] bits [3:0] REG[42h] bits [7:6]
Aspect Ratio Information: Other	Q0	xb	xb	xb	xb	xb	1b	xb		0b	0b	0b	0b	0b	0b	0b	1b	REG[44] bit 4	80h
End and Checksum	1b	1b	1b	1b	0b	0b	0b	1b		xb	xb	xb	xb	xb	xb	xb	xb	8Fh	Checksum Byte
XDS Start Current Program: CGMS (Analog)	1b	0b	0b	0b	0b	0b	0b	0b		1b	0b	0b	1b	0b	0b	0b	1b	01h	08h
CGMS (Analog)	ASB	APS B0	APS B1	CGMS -A B0	CGMS -A B1	0b	1b	xb		Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	1b	REG[46h] bits [1:0] REG[44h] bits [7:5]	REG[46h] bits [7:2]
End and Checksum	1b	1b	1b	1b	0b	0b	0b	1b		xb	xb	xb	xb	xb	xb	xb	xb	8Fh	Checksum Byte
Zero Data Dummy	0b	0b	0b	0b	0b	0b	0b	1b		0b	0b	0b	0b	0b	0b	0b	1b	80h	80h

Note
1. This bit is Reserved

19.2 CEA-608-B Manual Mode

The host has direct control of the VBI data and timing. Therefore, the user can support sending any type of data to conform with the CEA-608-B standard. In this mode, the host programs registers REG[42h] ~ REG[48h] only during the TV frame vsync time, so that the data will be sent out on the beginning of the upcoming field. This is accomplished by polling REG[4AEh] bit 4. After programming the data the host can trigger the VBI data to output on the specified field by writing a 1b to REG[4Ah] bit 3 and/or bit 2.

20 Typical Use Case Descriptions

20.1 Initializing the S1D13746

The S1D13746 is initialized based on the frequency of the input clock used for CLKI. CLKI is used as the source for the PLL and also can be used as the source for the TV Timing clock and the TV DDS clock. For further details on the S1D13746 clocks, see Section 9, “Clocks” on page 59.

The following steps are required to initialize the S1D13746.

- set the M-Divide which control the divide ratio between the CLKI input and the input clock to the PLL
- set the L-Counter which determines the output frequency of the PLL, in MHz
- set the TV Timing clock source
- set the TV DDS clock source
- disable sleep mode
  - The PLL must be correctly configured before disabling sleep mode
- check whether the PLL output is stable
  - This step must be performed before the synchronous registers can be accessed
- select the TV input clock settings which configures the clocks required for the TV block
- program the image data for display on the TV (see Section 20.2, “Writing An Image For Display On The TV” on page 163)
- enable the TV interface

For a example programming flows, see Section 20.1.1, “Initialization Flow Charts” on page 160.

20.1.1 Initialization Flow Charts

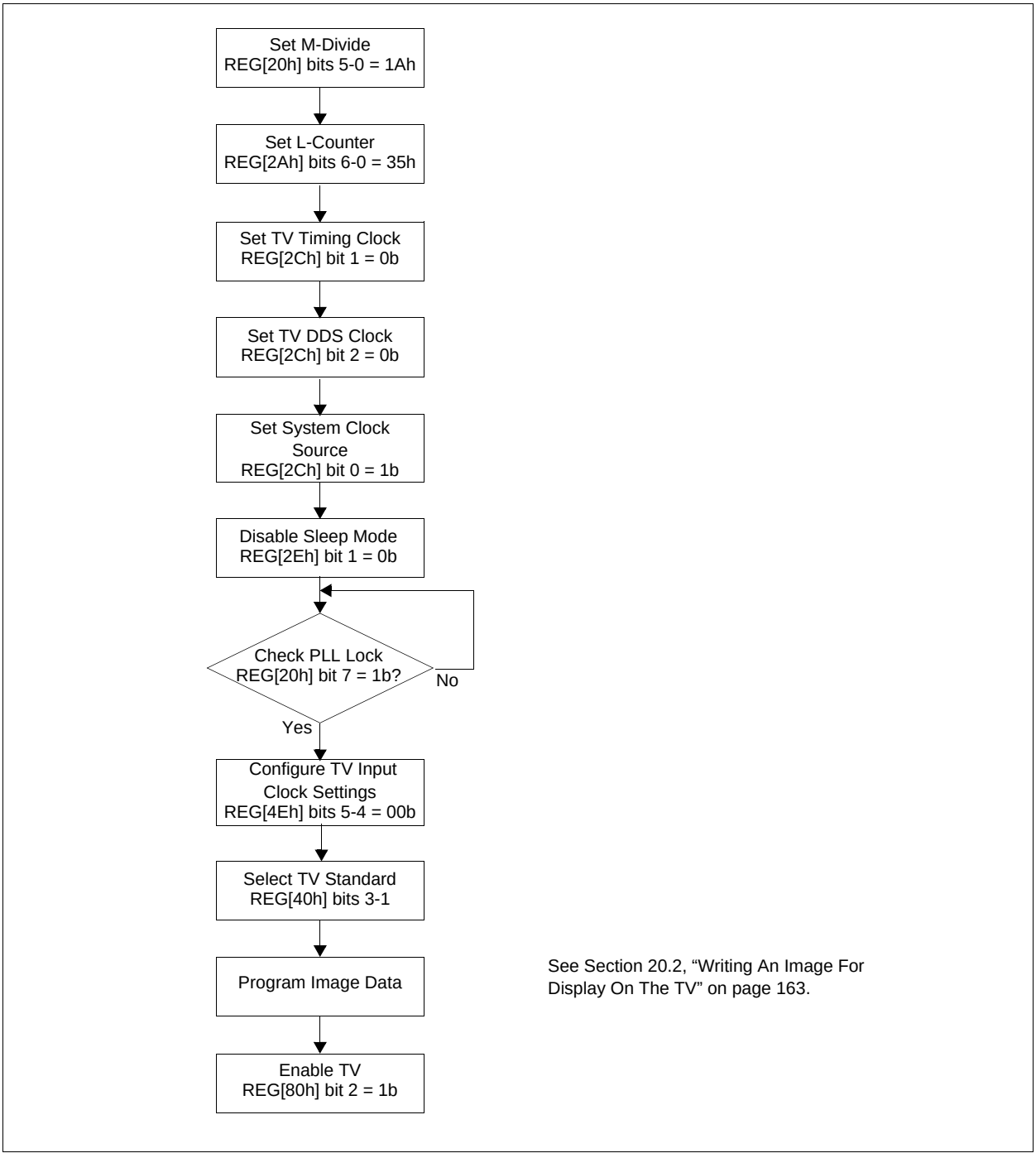


Figure 20-1: Initializing the S1D13746 for CLKI = 27MHz

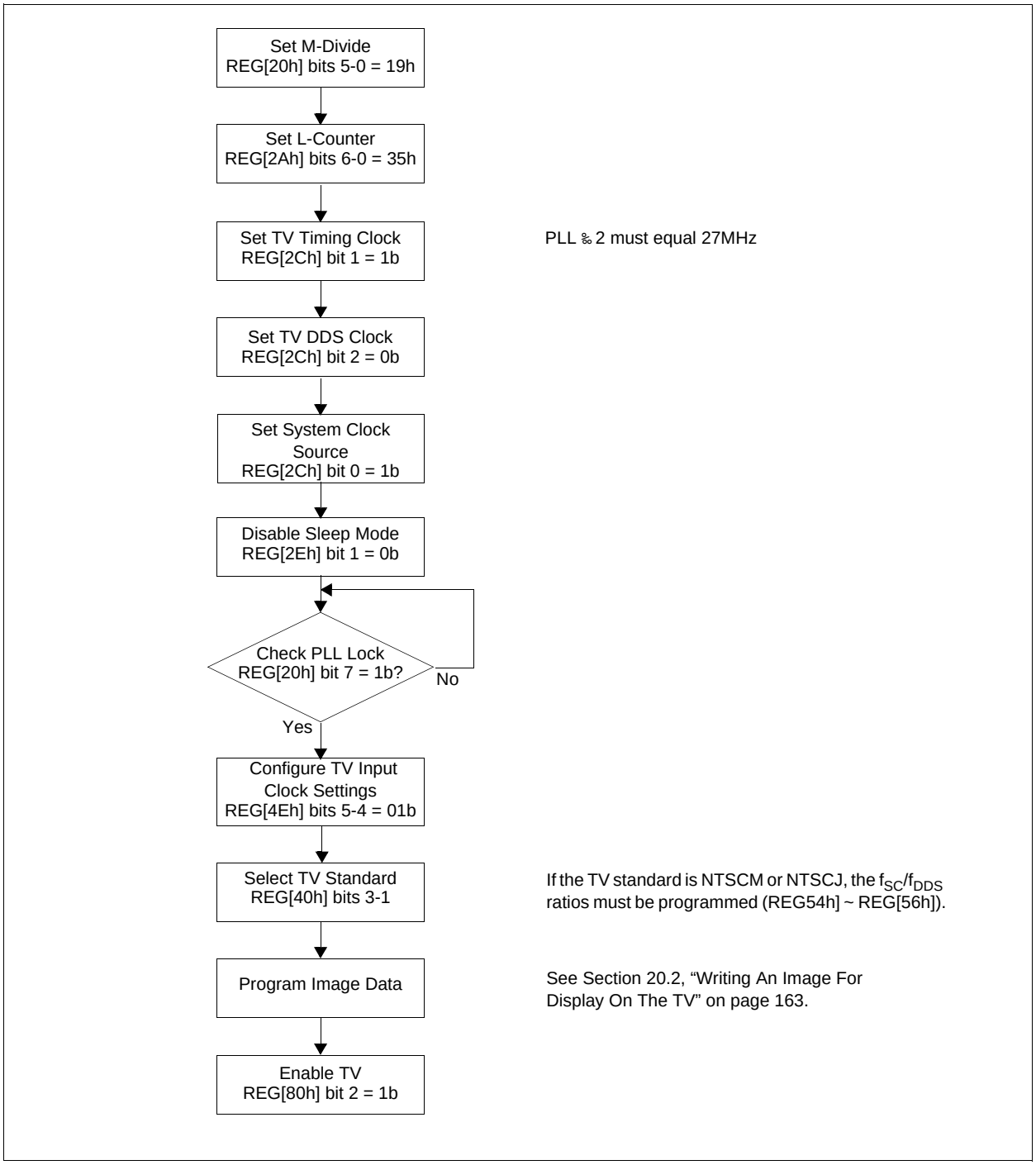


Figure 20-2: Initializing the S1D13746 for CLKI = 26MHz

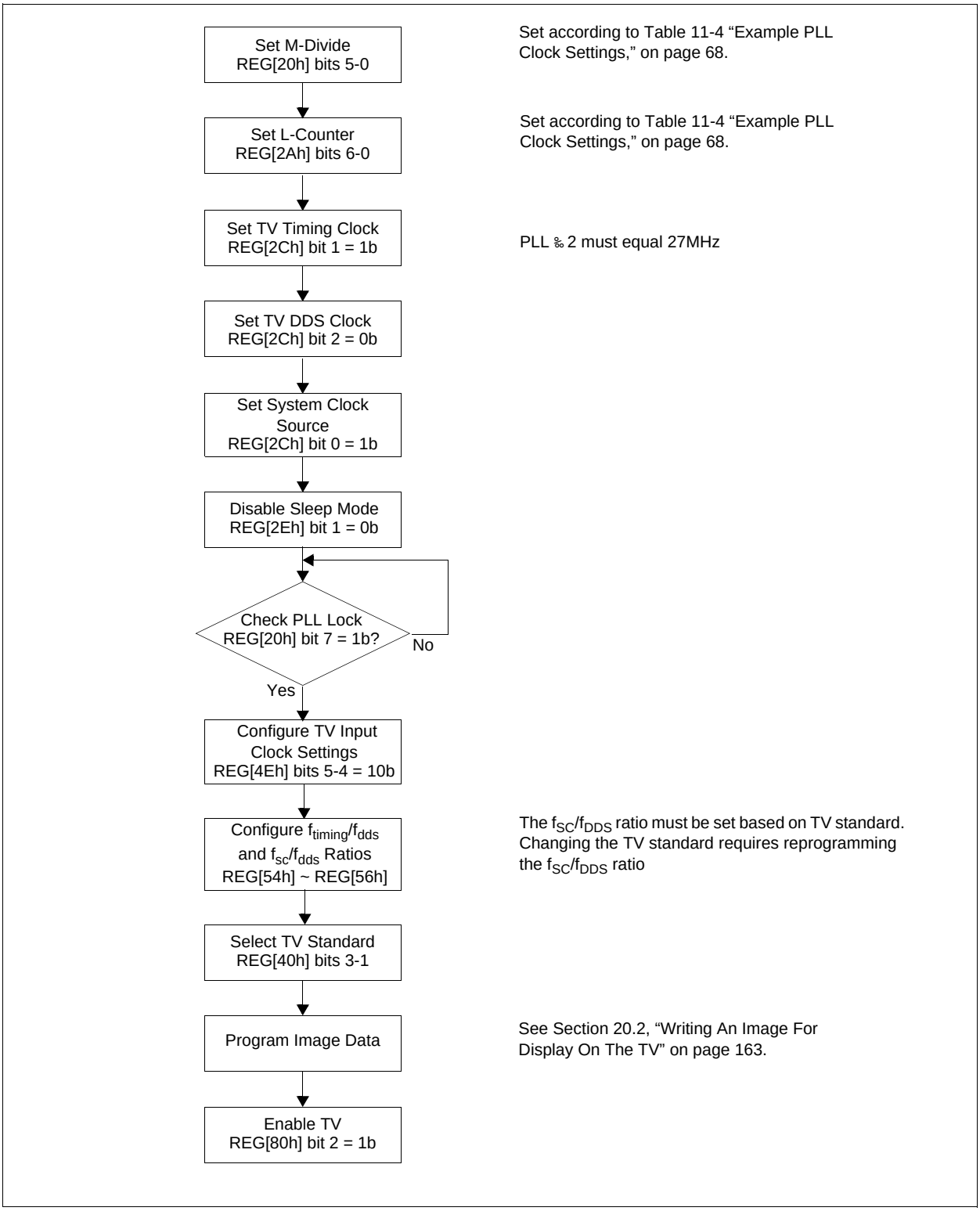


Figure 20-3: Initializing the S1D13746 for 18MHz ƒ CLKI ƒ 27MHz

20.2 Writing An Image For Display On The TV

If writing a single or multiple images on the display, one of them must be considered the "Background Image" (REG[62h] bit 5). The Input Scale Ratio is automatically calculated to allow this background image to fit in the available memory. All subsequent input images intended to be displayed on-top as overlays automatically use the same input scale ratio to maintain aspect with the background.

- set the Host Input Data Format
- set the Special Effects register as appropriate. If changing the Window Data Type from Streaming to Static while the double buffer remains enabled, then the Special Effects register should be set after the Host Input Size and Display Output Size and Positions registers.
  - Window Data Type
  - Background Image (if it is the background image, the automatic input scale ratio is latched and used for all subsequent images)
  - Double Buffer
  - Transparency
  - Window Rotation
- set the Host Input size
- set the Display Output Size/position accordingly
  - if the window being written is the background image, the Output position registers must be set to 0.
  - if the window being written is an overlay, the Output Height/Width registers are ignored.
  - if the window is the background and the Display Output Size does not equate to full-screen resolution as determined by PAL or NTSC, a Border is automatically generated.
- write window data

20.3 Use Case Flowcharts

20.3.1 Host Write Background

The following flowchart provides an example method for programming a static background window. This method can be used to program the background image when initializing the device, or any time the entire background must be re-painted. If the background must be re-programmed using different input/output coordinates, the display should be blanked before setting the new coordinates using the TV Display Blank bit, REG[80h] bit 3.

If a streaming background window is required, refer to Figure 20-6: “Streaming Background,” on page 166.

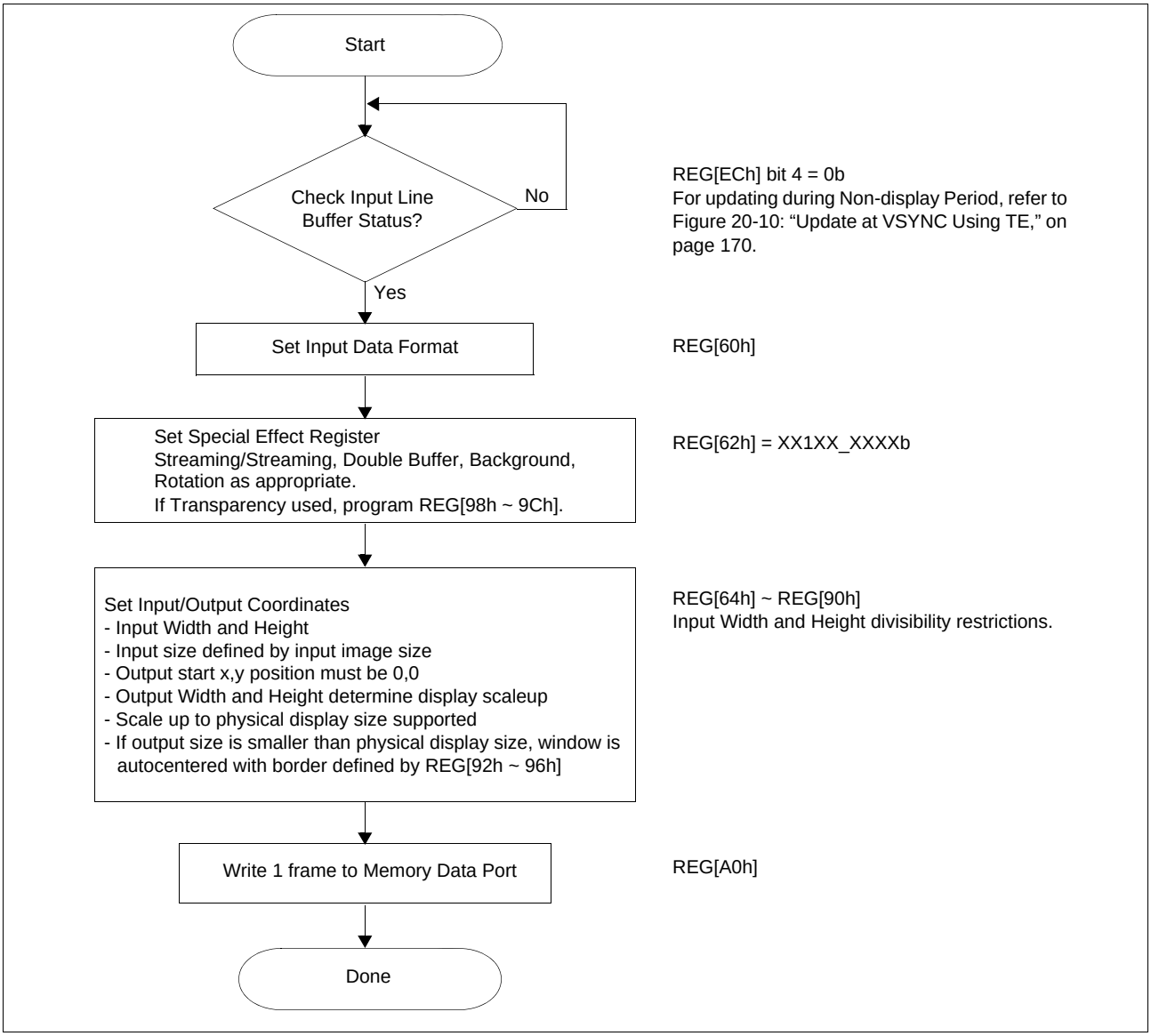


Figure 20-4: Host Write Background

20.3.2 Host Write Overlay

The following flowchart provides an example method for programming a static overlay window. The background window should be configured and programmed before an overlay window is programmed, as the scaling ratio from the background window is also used to scale the overlay window.

If a streaming overlay window is required, refer to Section 20.3.4, “Background and Streaming Overlay” on page 167.

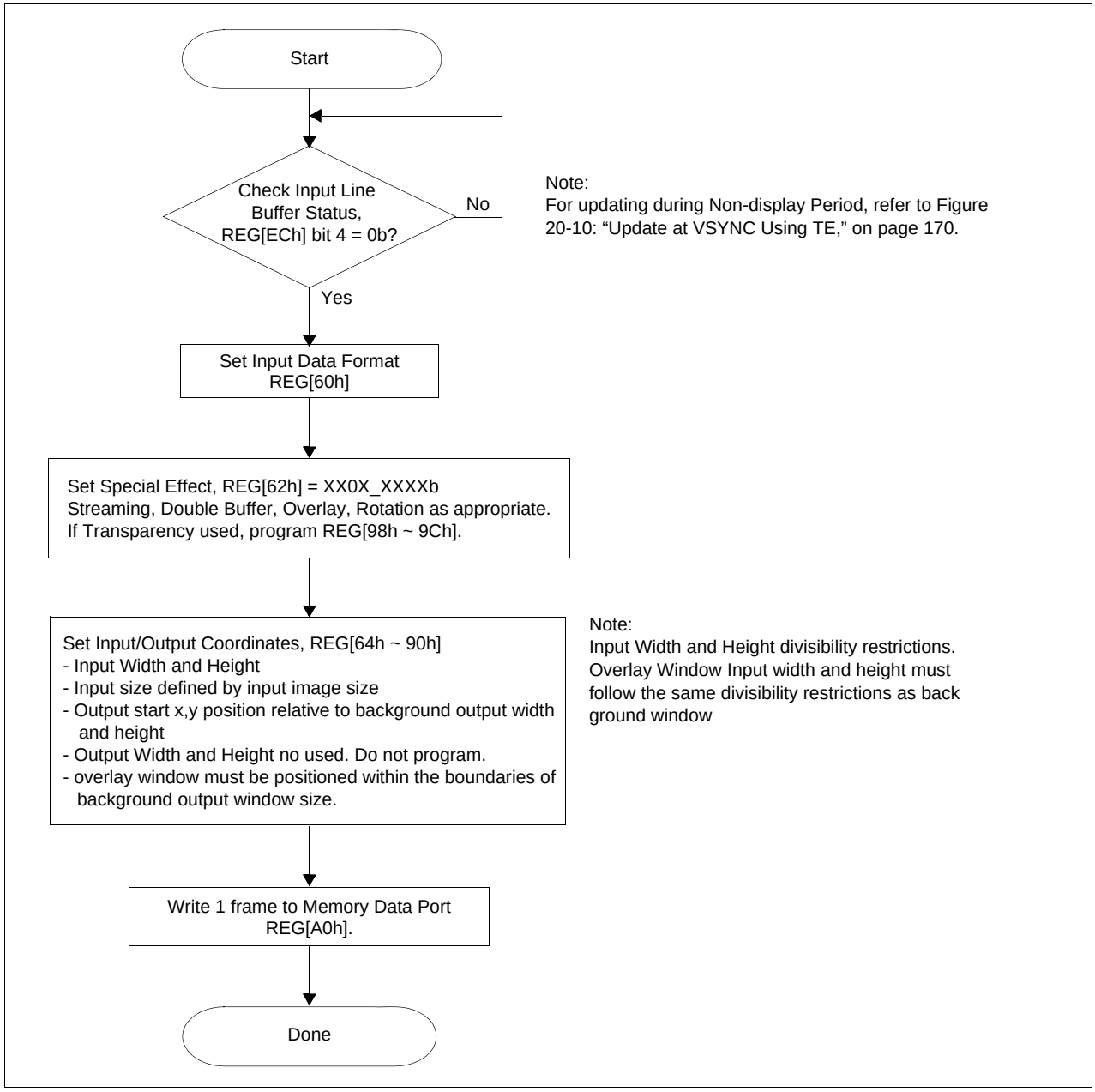


Figure 20-5: Host Write Overlay

20.3.3 Streaming Background

The following flowchart provides an example method for programming a streaming background window. This method should be used when the background image will be continually updated. If the background must be re-programmed using different input/output coordinates, the display should be blanked before setting the new coordinates using the TV Display Blank bit, REG[80h] bit 3.

If a static background window is required, refer to Figure 20-4: "Host Write Background," on page 164.

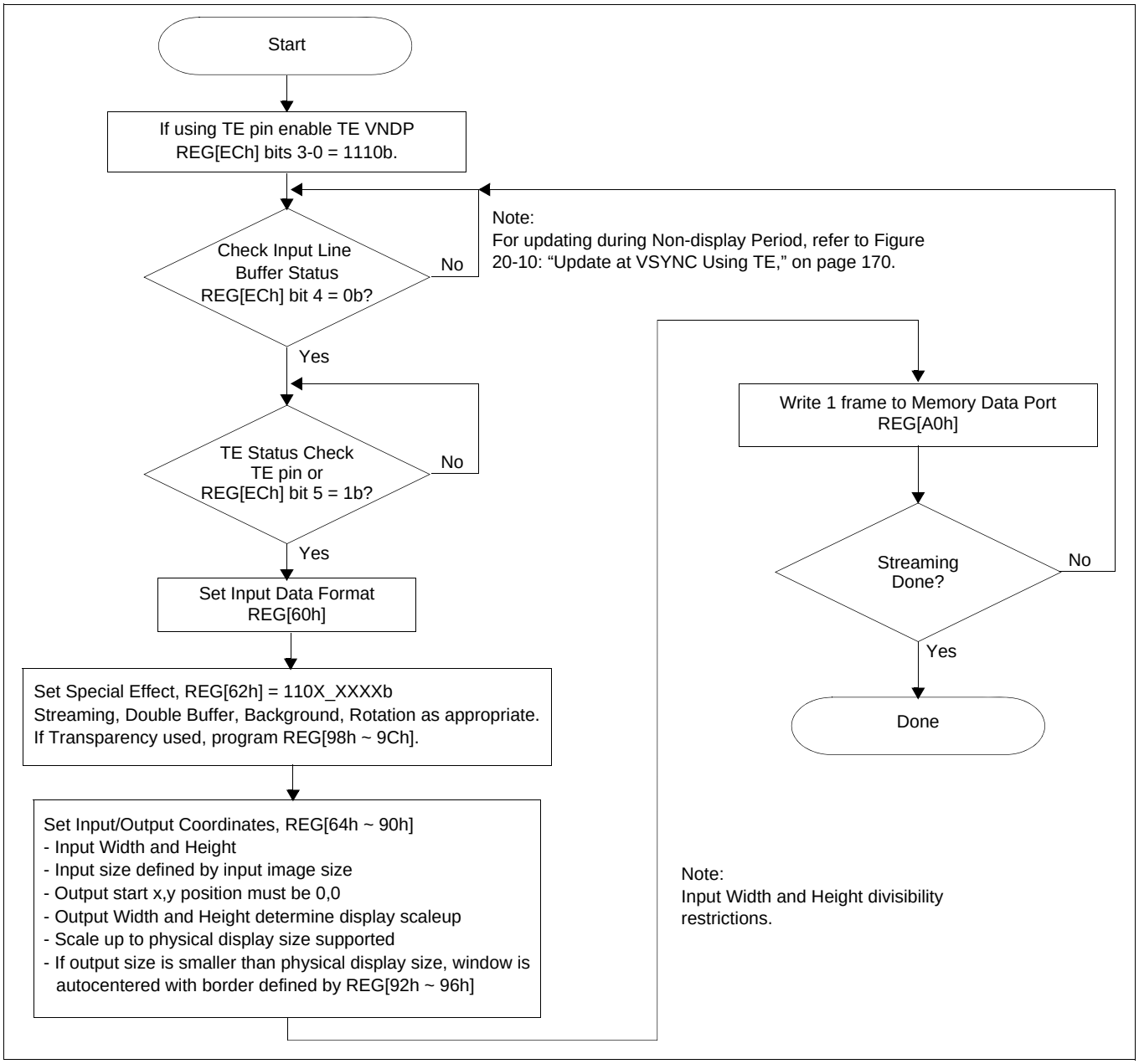


Figure 20-6: Streaming Background

20.3.4 Background and Streaming Overlay

The following flowchart provides an example method for programming a static background with a streaming overlay window.

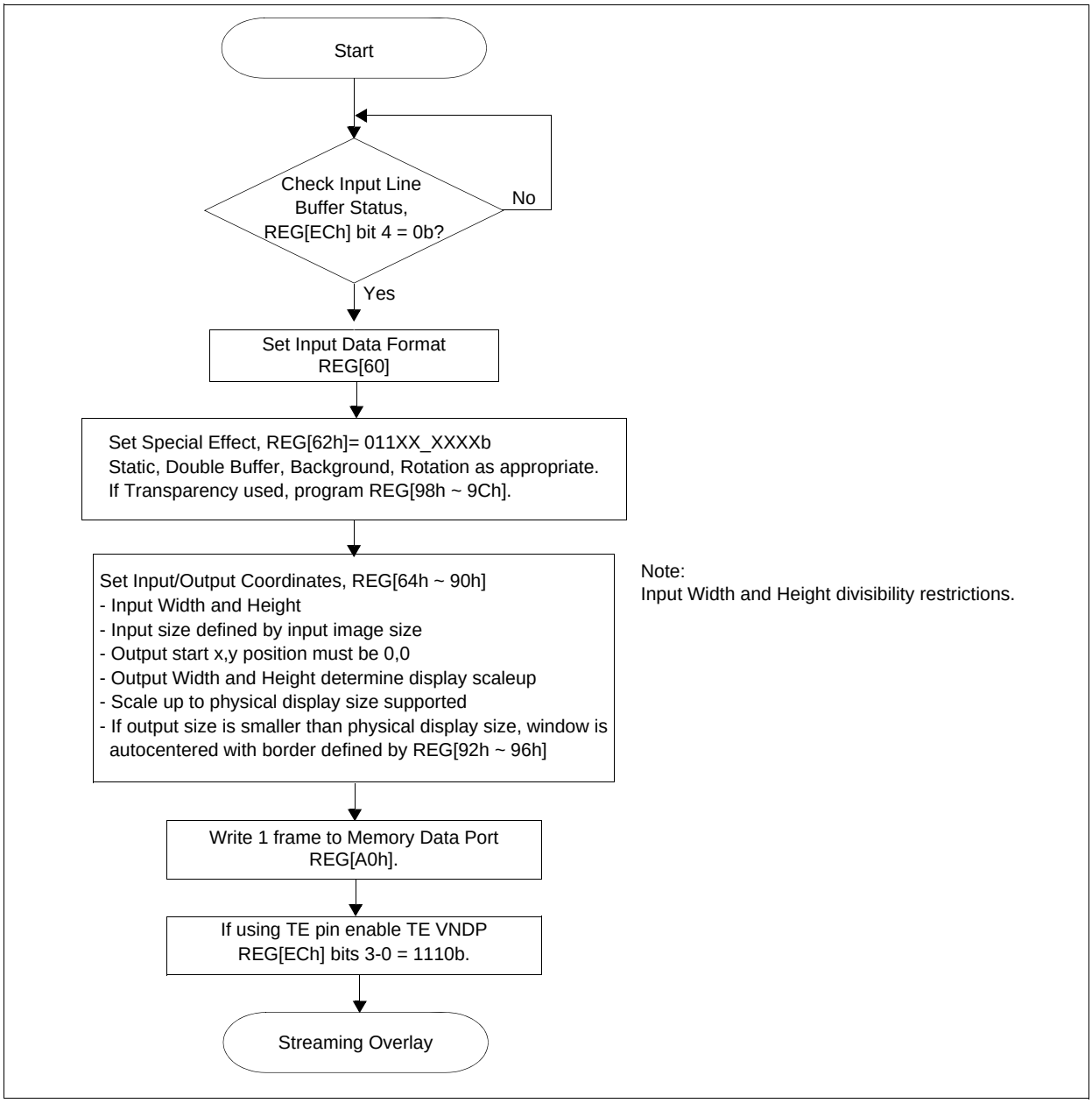


Figure 20-7: Background and Streaming Overlay (Figure 1 of 3)

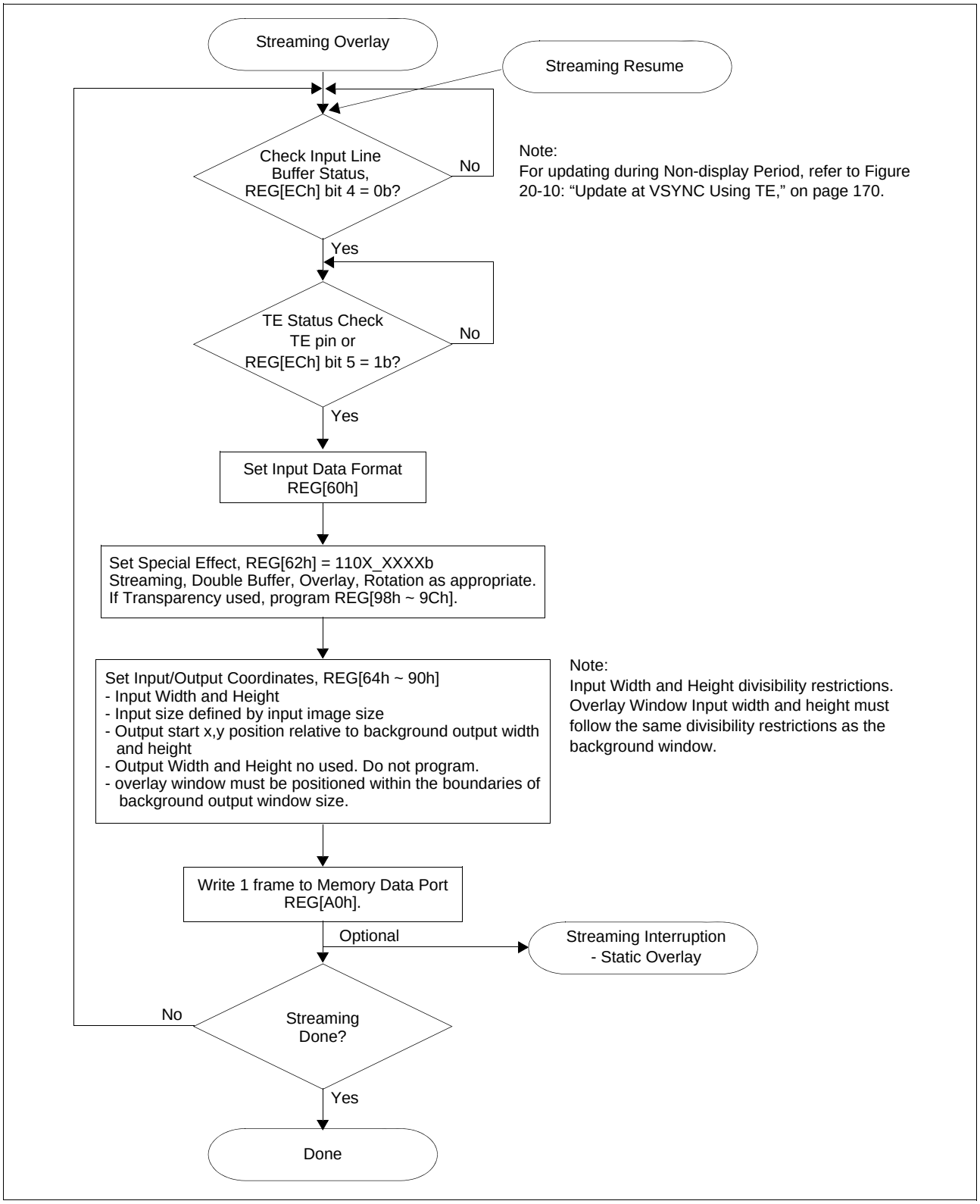


Figure 20-8: Background and Streaming Overlay (Figure 2 of 3)

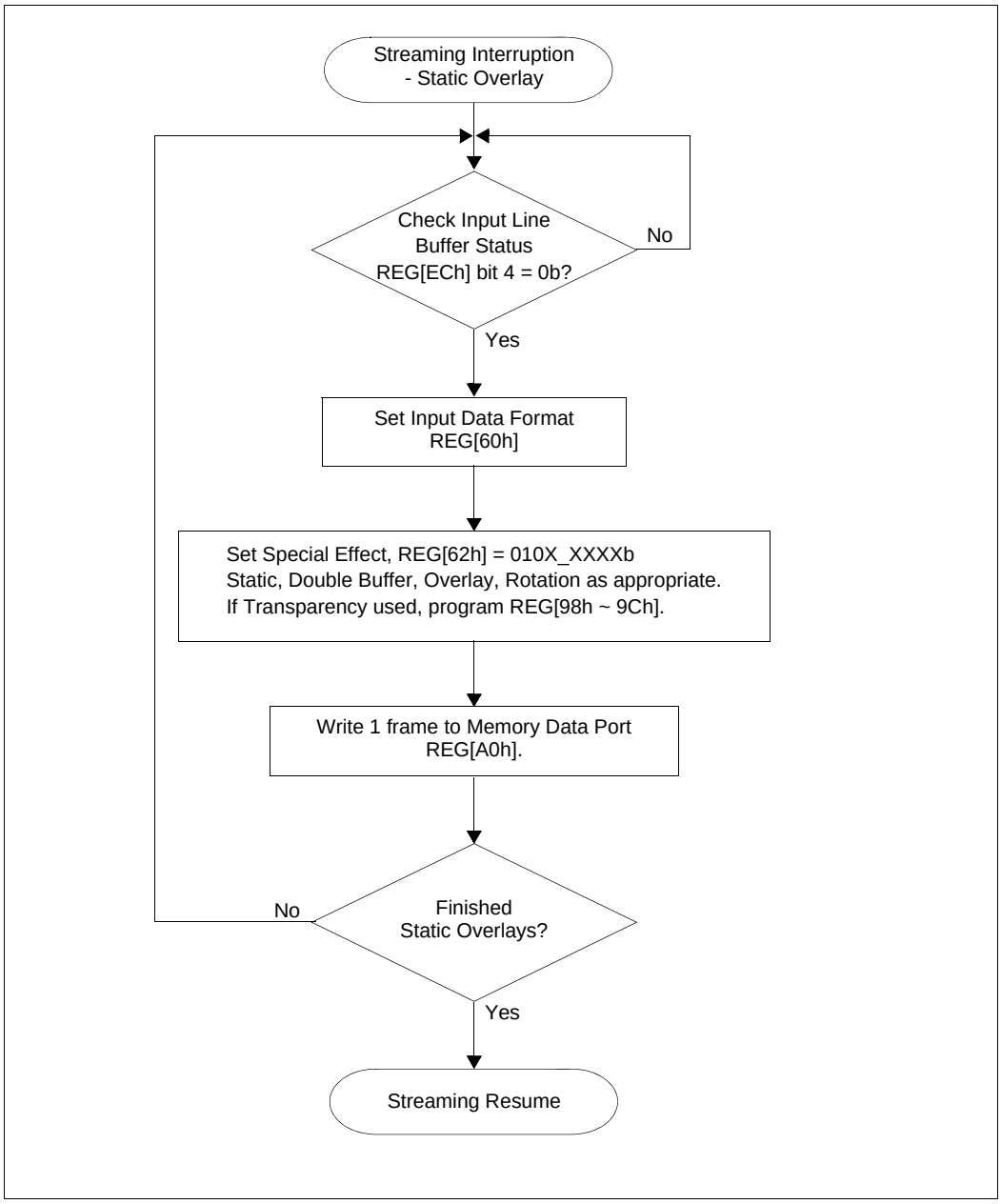


Figure 20-9: Background and Streaming Overlay (Figure 3 of 3)

20.3.5 Update at VSYNC Using TE

The following flowchart provides an example of how to use TE to perform updates during the VNDP. For further information on using TE and the various options available, refer to the bit descriptions in REG[ECh] (see Section 11.3.8, “Miscellaneous Registers” on page 114).

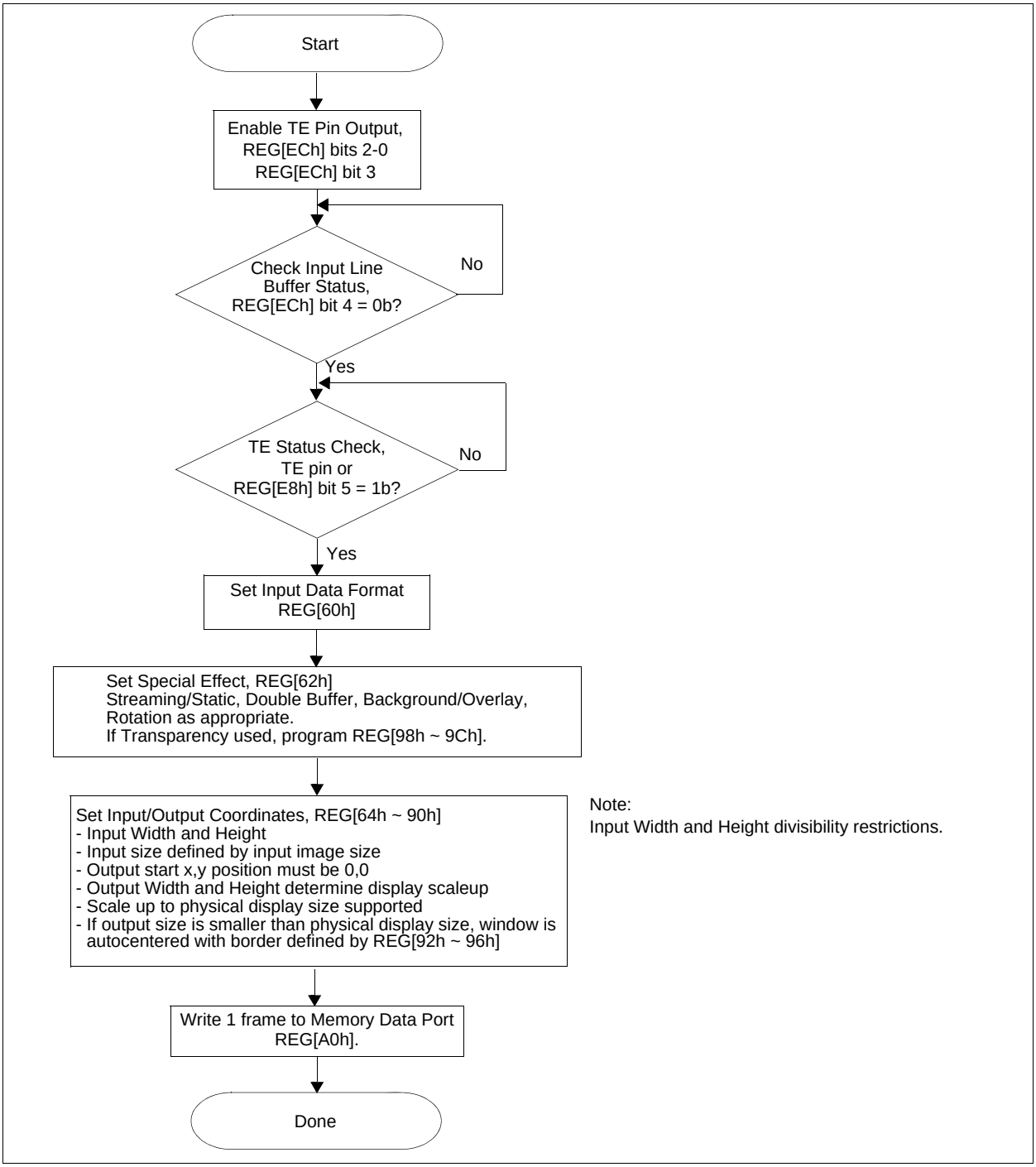


Figure 20-10: Update at VSYNC Using TE

20.4 Example: Enable a Double-Buffered Window on TV

This example shows how to open a destructive window and treat that window as double-buffered to accept a streaming input. It will also show how that window can be disabled such that the User Interface (static background image) can be updated

Write Background Window

- set the Input Data Format
- set the Special Effects register as appropriate
  - Window Rotation
  - Double Buffer Enable = 1
  - Window Data Type = 0
- set the Host Input Size and Display Output Size/Position
- write the background window data
- wait for the Input Busy Status = 0

Write Streaming Window

- set the Input Data Format
- set the Special Effects register as appropriate
  - Window Rotation
  - Double Buffer Enable = 1
  - Window Data Type = 1
- set the Host Input Size and Display Output Position
- write the streaming window data continuously (must ensure Input Busy Status = 0 between frames)

Interrupt Streaming to Update Static Data

- set the Input Data Format
- set the Host Input Size and Display Output Position
- set the Special Effects register as appropriate
  - Window Rotation
  - Double Buffer Enable = 1
  - Window Data Type = 0
- write the static data
  - wait for Input Busy Status = 0

Continue Writing Streaming Data

- set the Input Data Format
- set the Special Effects register as appropriate
  - Window Rotation
  - Double Buffer Enable = 1
  - Window Data Type = 1
- set the Host Input Size and Display Output Position
- write the streaming window data continuously (must ensure Input Busy Status = 0 between frames)

Note

S1D13746 utilizes a double buffer architecture to prevent any visual tearing during streaming input. The active display pipe only reads from a buffer after it has been completely written. At this time, the host writes switches to the other buffer. If necessary, the TE output pin can be used in conjunction with double buffering to guarantee that no tearing will occur.

21 Double Buffer Description

Double buffering is provided to prevent tearing of streaming video data. All static (non-video) image data will always be written to Buffer 1 of the frame buffer. When video is being input, the frame will be written alternately between Buffer 2 and Buffer 1. While video data is being input, the static part of the image going to the TV will still always come from Buffer 1. The source of the streaming video window will come from either Buffer 1 or Buffer 2, depending on which one was the last to be completely updated.

When streaming video data, each time the user finishes writing a frame of video data, they should wait until the ILB (Input Line Buffer) is not busy and for the next vertical non-display period before writing the next frame. This can be accomplished by first polling ILB status (REG[EC] bit 4) and then using the TE pin or by polling the TE Status bit (REG[ECh] bit 5). Alternatively, if the user can guarantee that the maximum input video frame rate is one half the TV Field Rate (60Hz for NTSC and PAL-M, 50Hz for PAL) and that the burst length for writing a video frame is less than one TV Field Period, then no checking for the vertical non-display period is required.

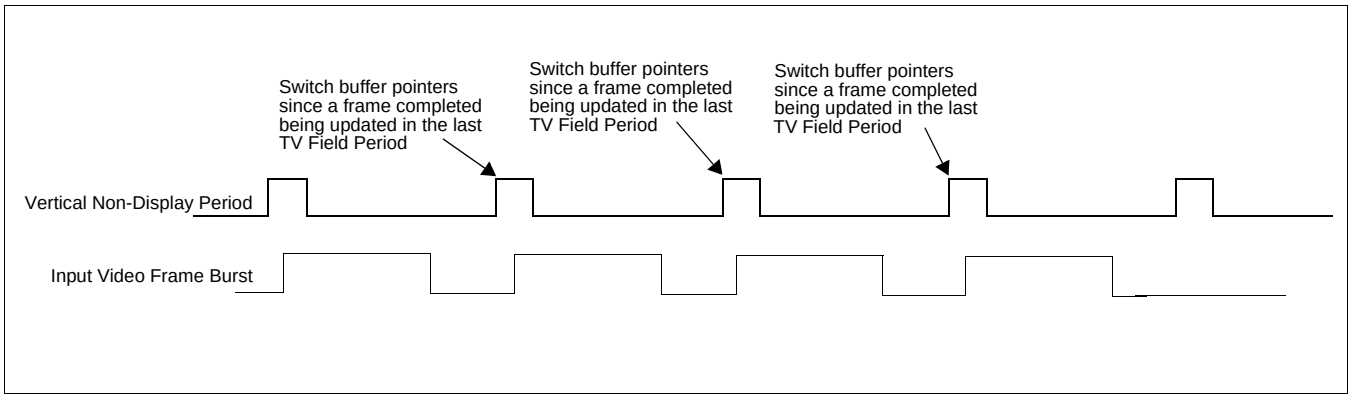


Figure 21-1: Double Buffer Streaming Timing - Recommended

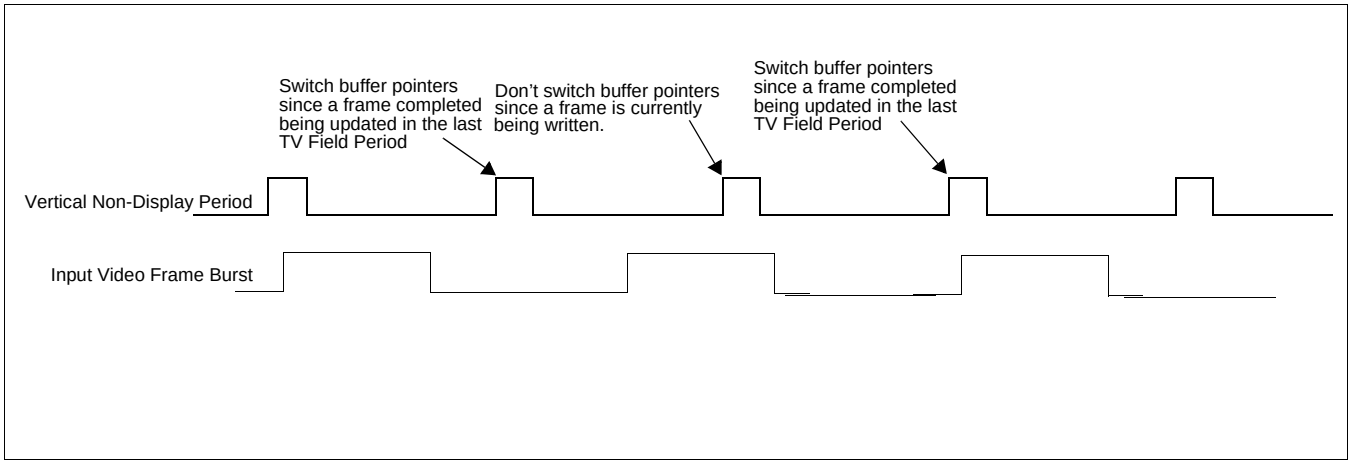


Figure 21-2: Double Buffer Streaming Timing - Not Recommended

To use the double buffer feature:

- Check the ILB Status, REG[EC] bit 4.
- Check TE VNDP Status, TE pin or REG[EC] bit 5.
- Set the Input Data Format REG[60].
- Set the Special Effects Register REG[62h] bits 7-6 to 11b.
- Setup the Host Window Size / Position registers (REG[64h] ~ REG[6Ah], REG[82h] ~ REG[90h].
- Write a frame of video data to the Memory Data Port REG[A0h].
- Repeat all check of ILB status and TE VNDP before writing each subsequent frame to Memory Data Port.

It is also possible to update a static window while double buffering is enabled, even in the middle of a video stream. To do this:

- Write the last pixel of the current frame of video data.
- Set the Special Effects Register REG[62h] bits 7-6 to 01b.
- Set the Input Data Format REG[60].
- Setup the Host Window Size / Position registers (REG[64h] ~ REG[6Ah], REG[82h] ~ REG[88h].
- Write the static data to the Memory Data Port REG[A0h].

This allows a static image to be written at any time, while still preventing the double buffered window from tearing. Once the static window has been written, the user can go back to writing the streaming video data by repeating the steps described above for using the double buffer feature.

21.1 Double Buffering Limitations

- When a streaming and static overlay window overlap and streaming is stopped, the streaming overlay window data will overwrite the static overlay window data if streaming is resumed.
- When a double buffered streaming overlay window is stopped and double buffering is disabled, the TV will display either the most recent frame or the previous frame to it.
- The user must either wait for a vertical non-display period between writing frames of video data, or guarantee that their maximum input frame rate is 1/2 the TV Field Rate (60Hz for NTSC and PAL-M, 50Hz for PAL) and that the length of time it takes to burst write a frame of video data is less than one TV Field Period.
- Only one window can be double buffered at a time.
- A double buffer streaming overlay window, requires the background window to be created with double buffer enabled.
- Input Line Buffer (ILB) Status must still be checked for idle before writing back to back frame data.

22 TV Filter Operation

The S1D13746 contains fixed and programmable digital filters to minimize noise in the TV luminance and chrominance signals. For the fixed filters setting (REG[52h] bit 2 = 0b), the function of the luminance filter depends on the current TV output type (REG[40h] bit 4) and the selected TV standard in REG[40h] bits 3-1.

For S-Video TV output, the fixed filter function for luminance is a 4MHz low pass filter. For Composite TV output, the fixed filter function for luminance is a notch filter at either 3.58 or 4.43 MHz depending on the TV standard setting (REG[40h] bits 3-1).

The fixed filter function for chrominance is a low pass filter with 1.5 dB attenuation at 1.3MHz and >20 db at 3.6 MHz.

The TV filters default functions will perform optimally in most cases. However, if the user wishes to optimize the filter performance further for their application, custom filter coefficients can be generated with generic FIR filter design software and programmed into indirect indexed registers REG[54h] and REG[56h].

22.1 Generating Custom Luminance (Y) and Color (UV) Filter Coefficients

The Luminance and Chrominance are symmetric FIR filters. The coefficient values can be positive or negative. See Figure 22-1: “15-Tap, Positive Symmetric Impulse Response,” on page 176.

For symmetric impulse response, only 8 of the coefficients are needed to be programmed as the remaining 7 are a duplicate of the first 7.

Similarly, the chrominance is a 15-Tap FIR filter similar to Figure 22-1: “15-Tap, Positive Symmetric Impulse Response”. For symmetric impulse response, only 8 of the coefficients are needed to be programmed as the remaining 7 are a duplicate of the first 7.

The coefficients are 2’s complement and 9-bits wide.

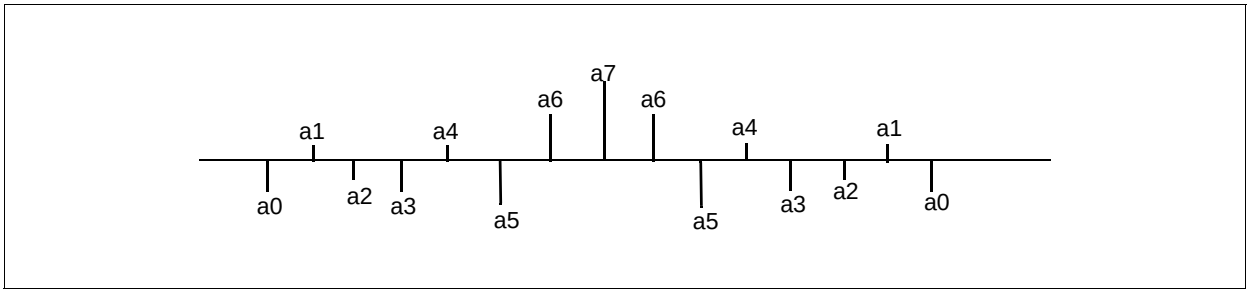


Figure 22-1: 15-Tap, Positive Symmetric Impulse Response

22.1.1 Filter Parameters

The following information is required in order to generate custom FIR filter values. However, it will depend on the users filter design software and is provided as a guide.

- type of filter: low pass, high pass, notch, band stop
- sample clock frequency: 13.5 MHz (fixed)
- number of taps: 15 (Y) and 15 (UV)
- upper pass band, i.e. 4 MHz
- stop band, i.e. 6.2 MHz
- pass band ripple, i.e. 3 dB
- stop band attenuation, i.e. 60 dB

The below response curves show the theoretical performance of the built-in fixed function TV filter.

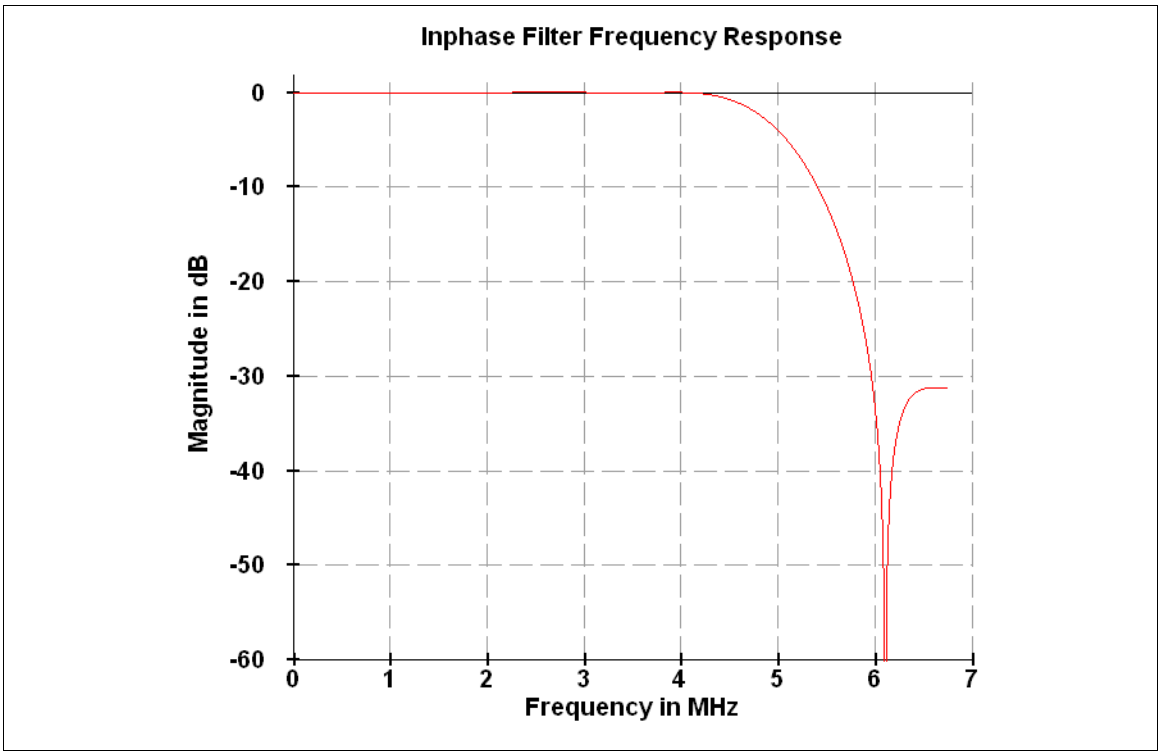


Figure 22-2: Frequency Response of Y 4MHz Low Pass Filter

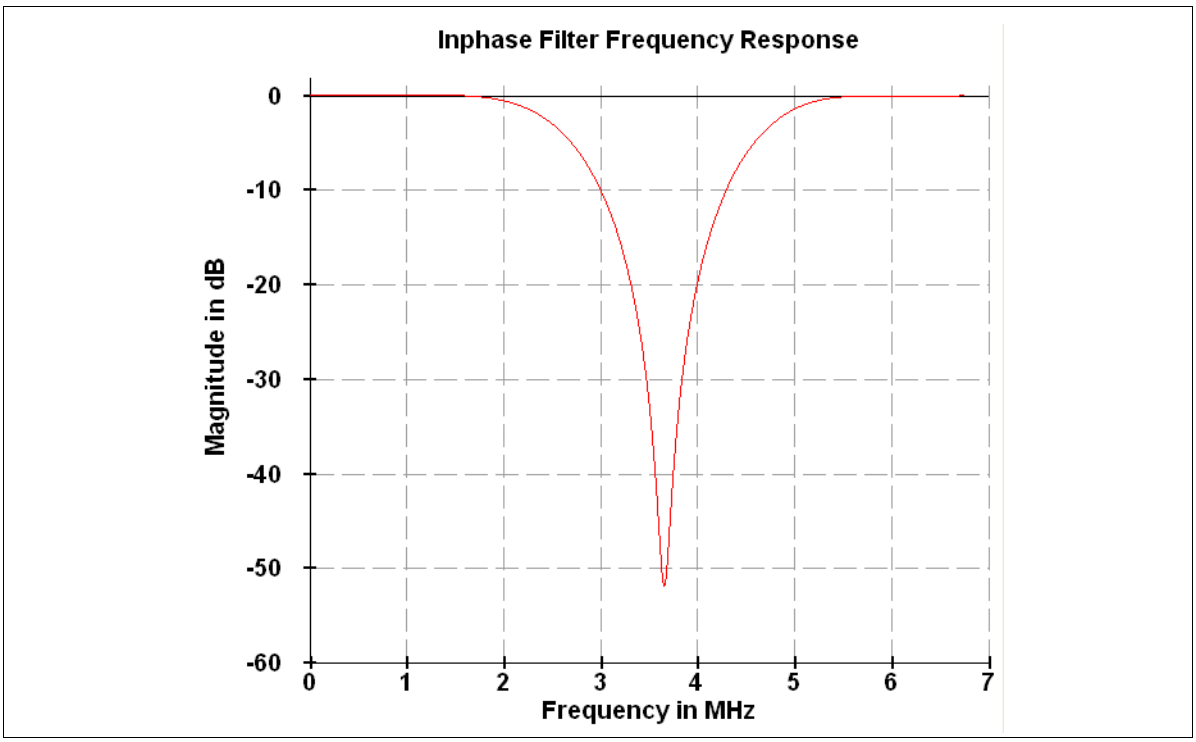


Figure 22-3: Frequency Response of Y Notch Filter @ 3.58MHz

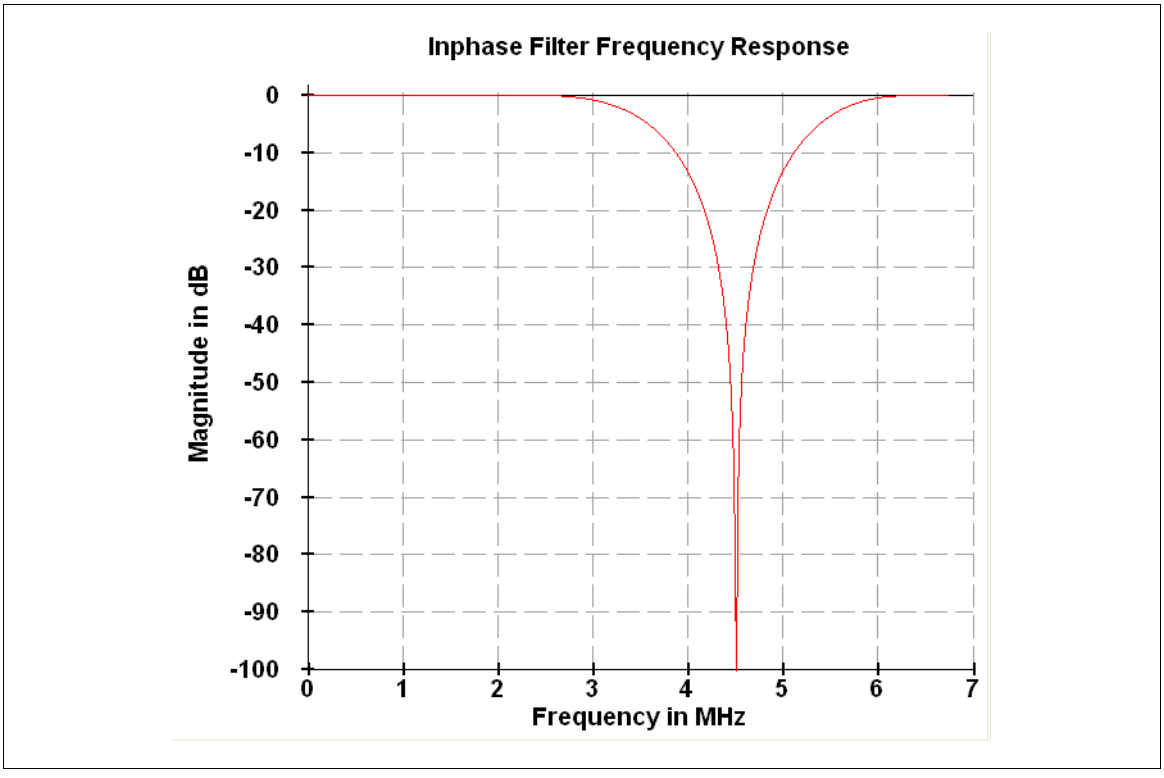


Figure 22-4: Frequency Response of Y Notch Filter @ 4.43MHz

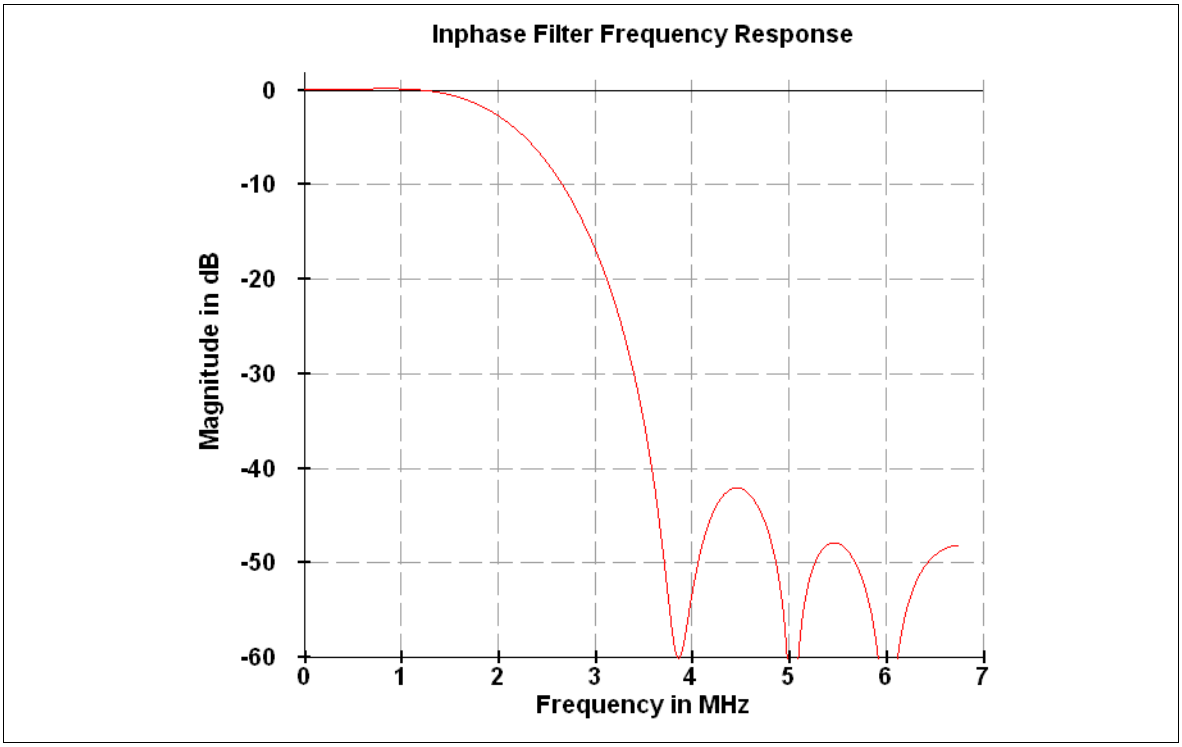


Figure 22-5: Frequency Response of UV Filter

23 Power Save Modes

The S1D13746 supports two power save modes: Sleep Mode and Standby Mode.

23.1 Sleep Mode

Sleep mode disables all internal blocks except the analog TV encoder block, which must be manually disabled before entering Sleep mode. This mode offers the lowest power consumption, but when Sleep mode is disabled the S1D13746 requires approximately 2.5ms before the PLL becomes stable. The S1D13746 should not be accessed during this period.

Sleep mode is controlled by the Sleep Mode Enable bit (REG[2Eh] bit 1) or the PWRSVE pin when REG[2Eh] bit 7 = 0b. For further details on Sleep Mode, refer to the bit description for REG[2Eh] bit 1 in Section 11.3.2, “Clock Configuration Registers” on page 66.

The following sequence is recommended for entering Sleep mode.

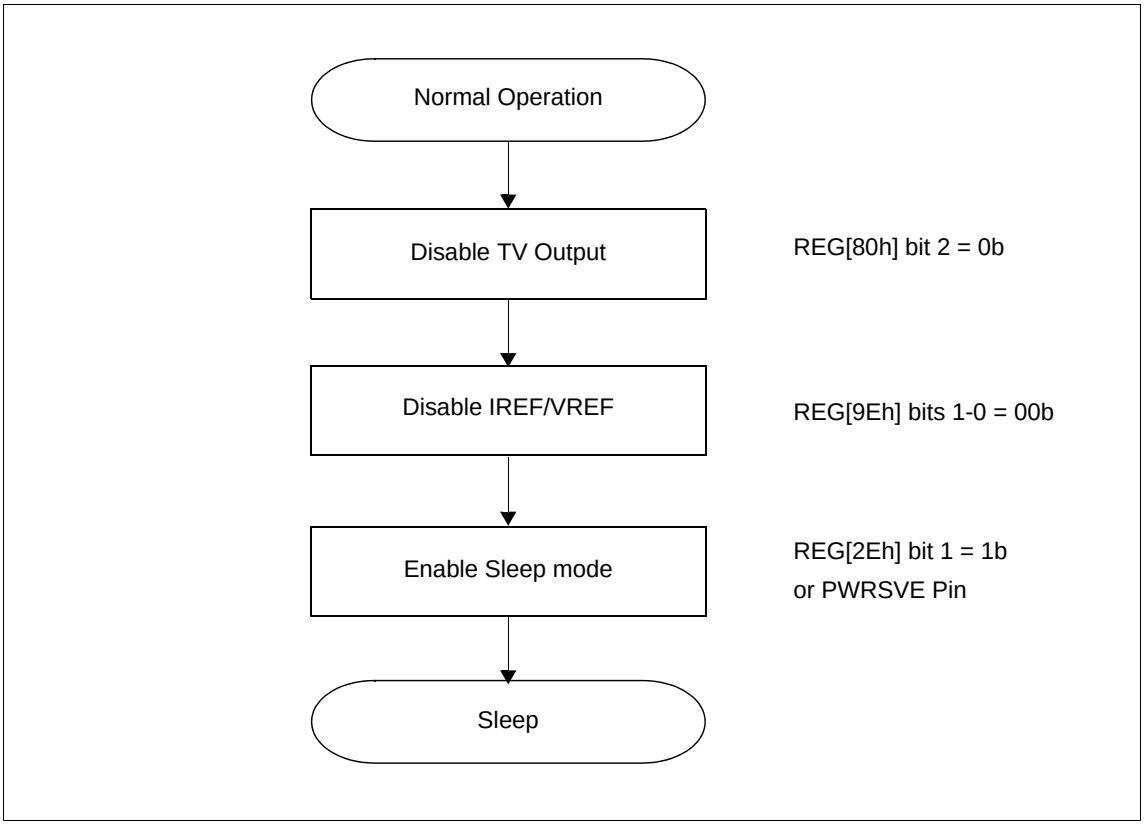


Figure 23-1: Recommended Sequence for Entering Sleep Mode

The following sequence is recommended for exiting Sleep mode.

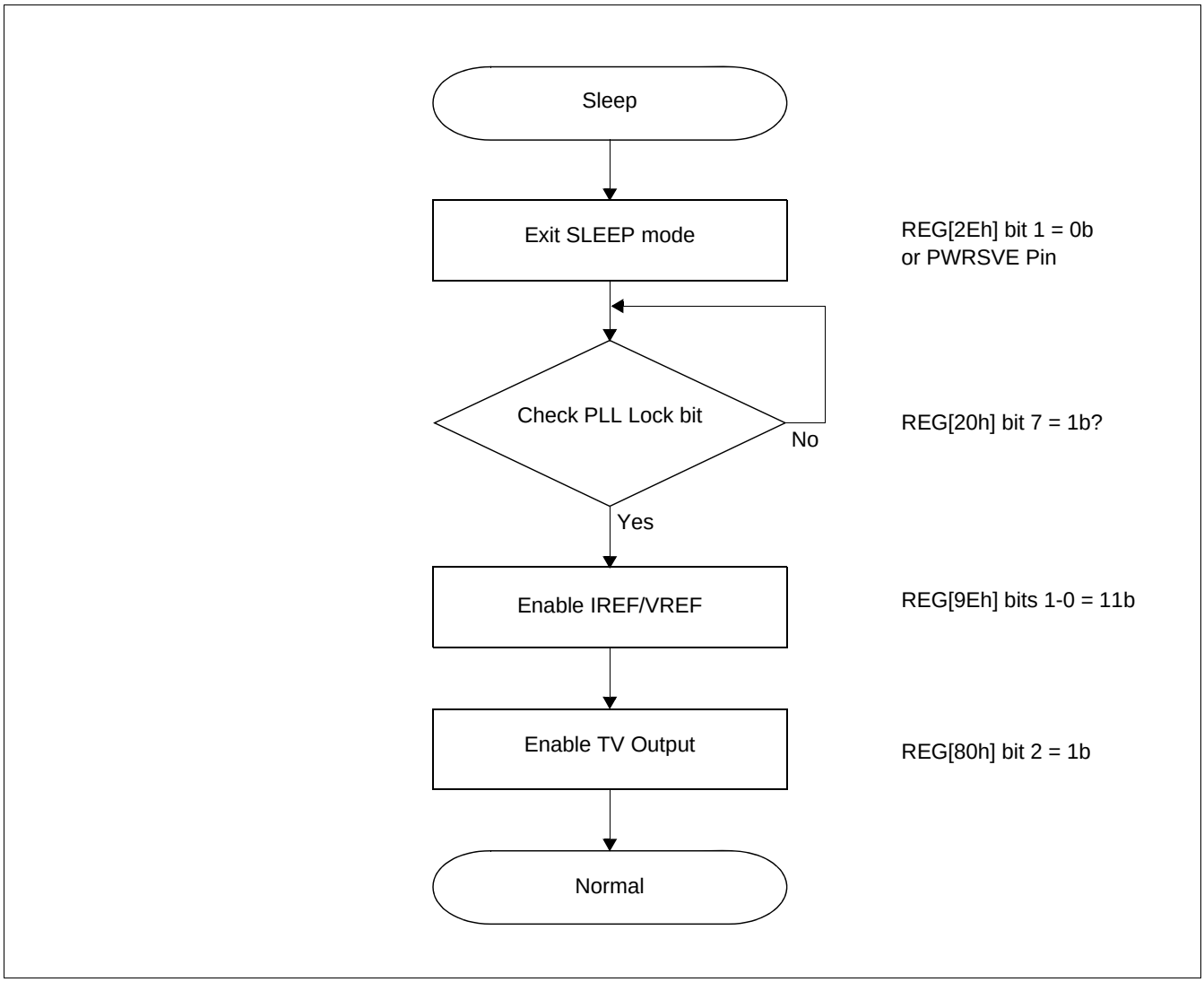


Figure 23-2: Recommended Sequence for Exiting Sleep Mode

23.2 Standby Mode

Standby mode disables all internal blocks except the PLL and analog TV encoder blocks. The analog TV encoder block must be manually disabled before entering Standby mode. This mode offers the advantage of being able to access the S1D13746 immediately after disabling Standby mode.

Standby mode is controlled by the Standby Mode Enable bit (REG[2Eh] bit 0) or the PWRSVE pin when REG[2Eh] bit 7 = 1b. For further details on Standby Mode, refer to the bit description for REG[2Eh] bit 0 in Section 11.3.2, “Clock Configuration Registers” on page 66.

The following sequence is recommended for entering Standby mode.

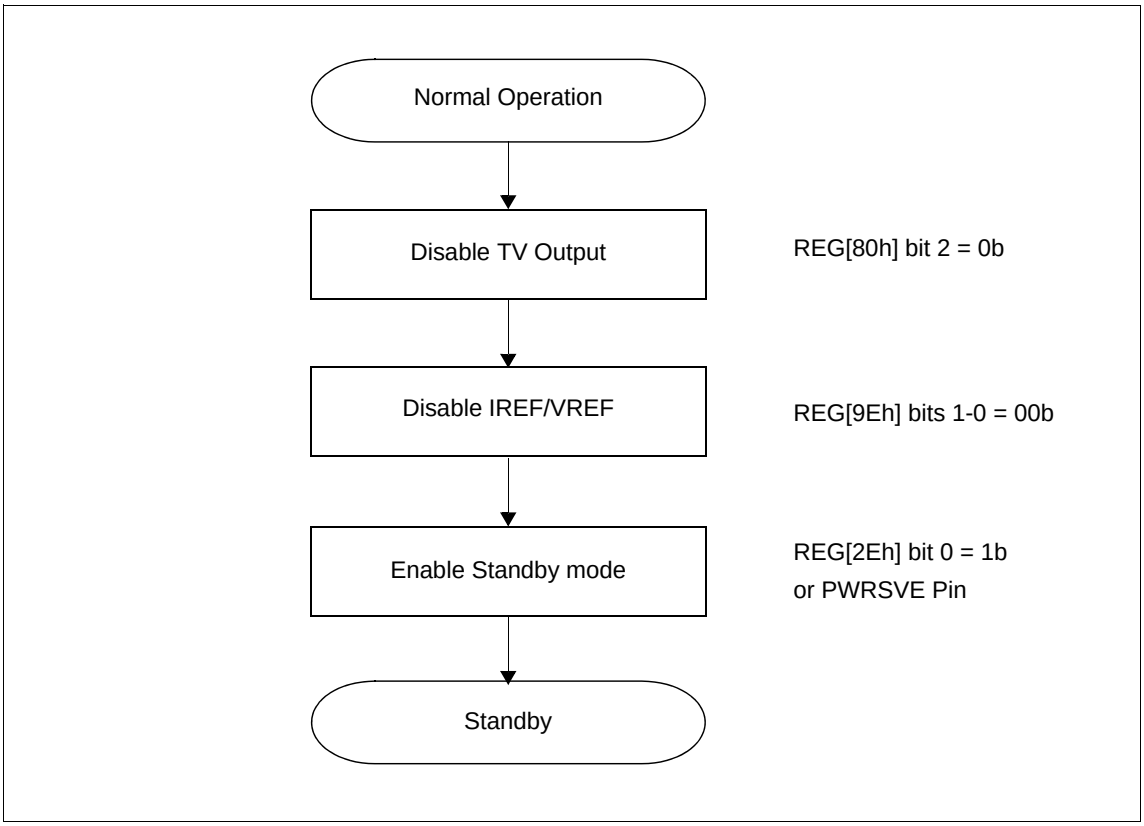


Figure 23-3: Recommended Sequence for Entering Standby Mode

The following sequence is recommended for exiting Standby mode.

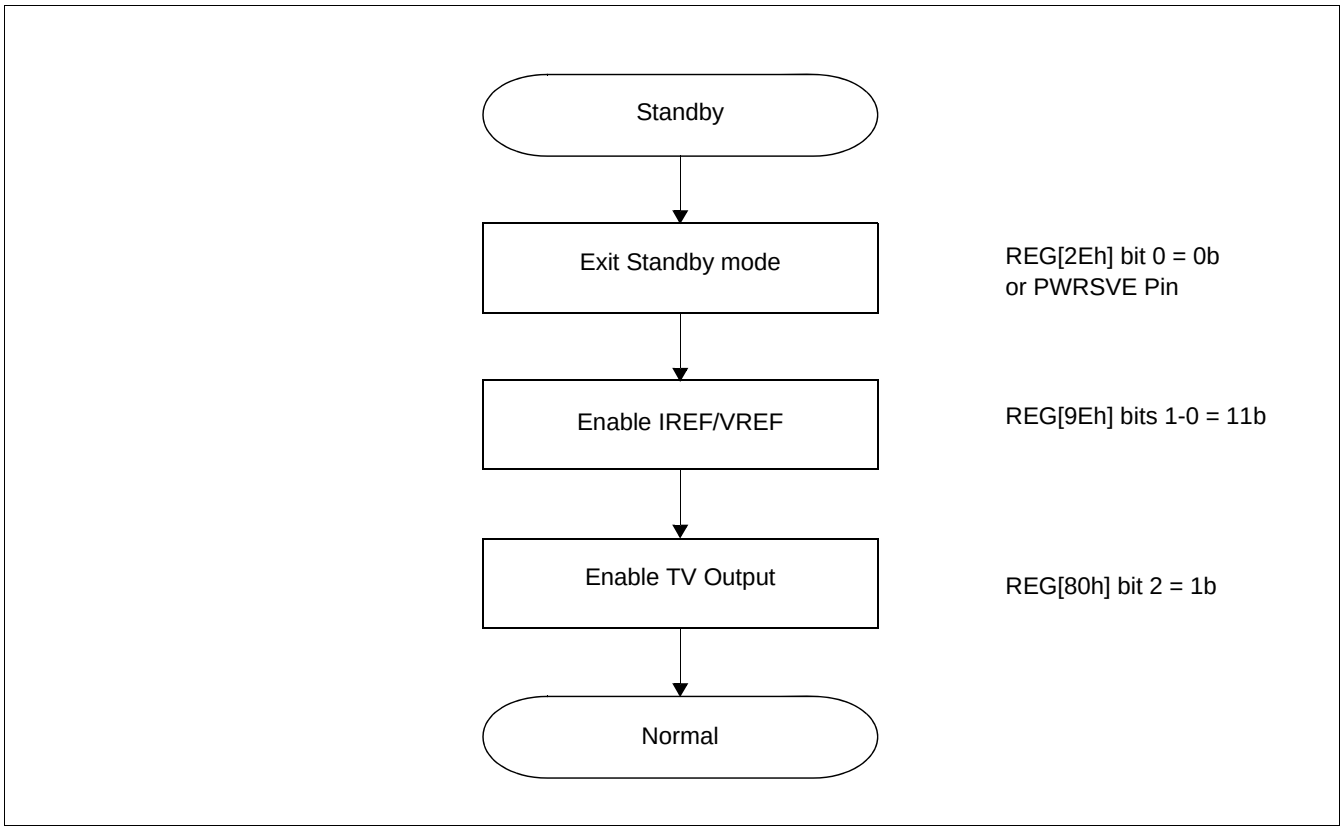


Figure 23-4: Recommended Sequence for Exiting Standby Mode

24 External Components

24.1 DAC External Components

The following circuit is recommended when Internal VREF is used, REG[9Eh] bit 0 = 1b

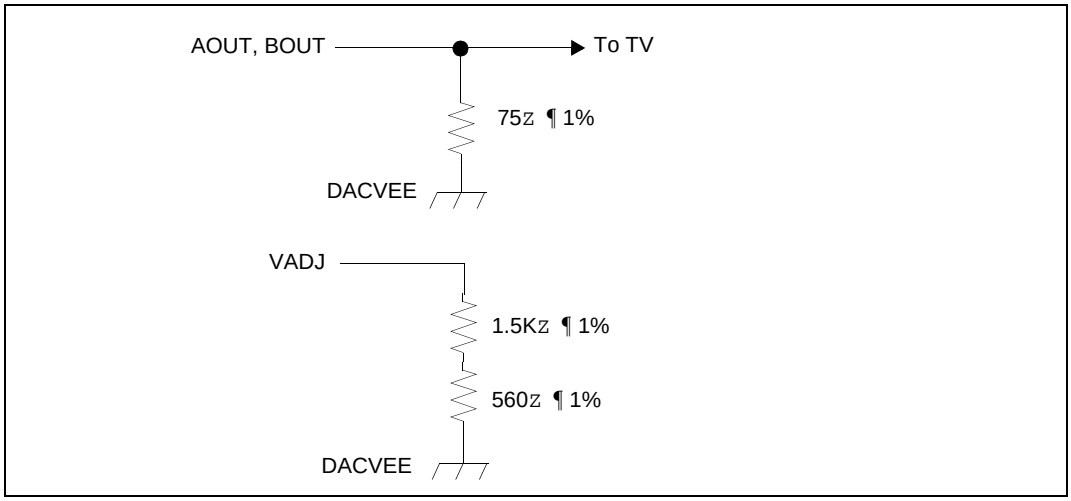


Figure 24-1: Recommended External Components - Internal V-Ref Used

The following circuit is recommended when External VREF is used, REG[9Eh] bit 0 = 0b

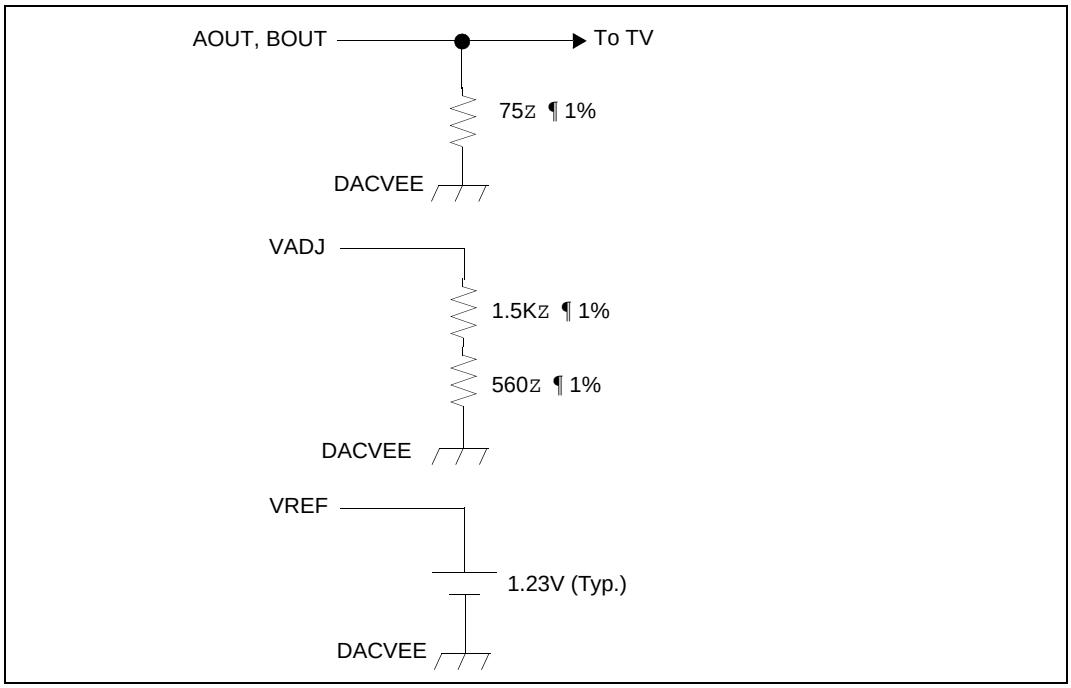


Figure 24-2: Recommended External Components - External V-Ref Used

The following circuit is recommended for the DAC power supply pins.

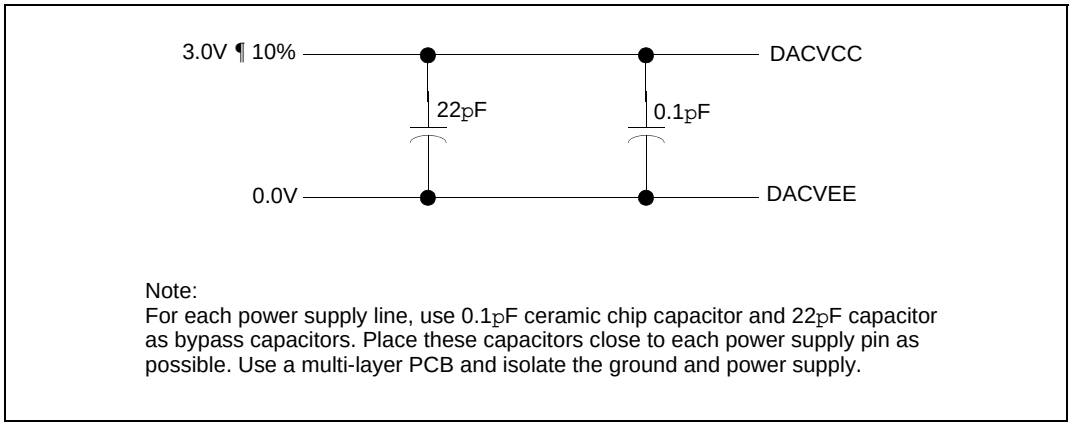


Figure 24-3: Recommended External Components - DAC Power Pins, ESD Considerations

The following circuit describes the recommended external components for TV analog output.

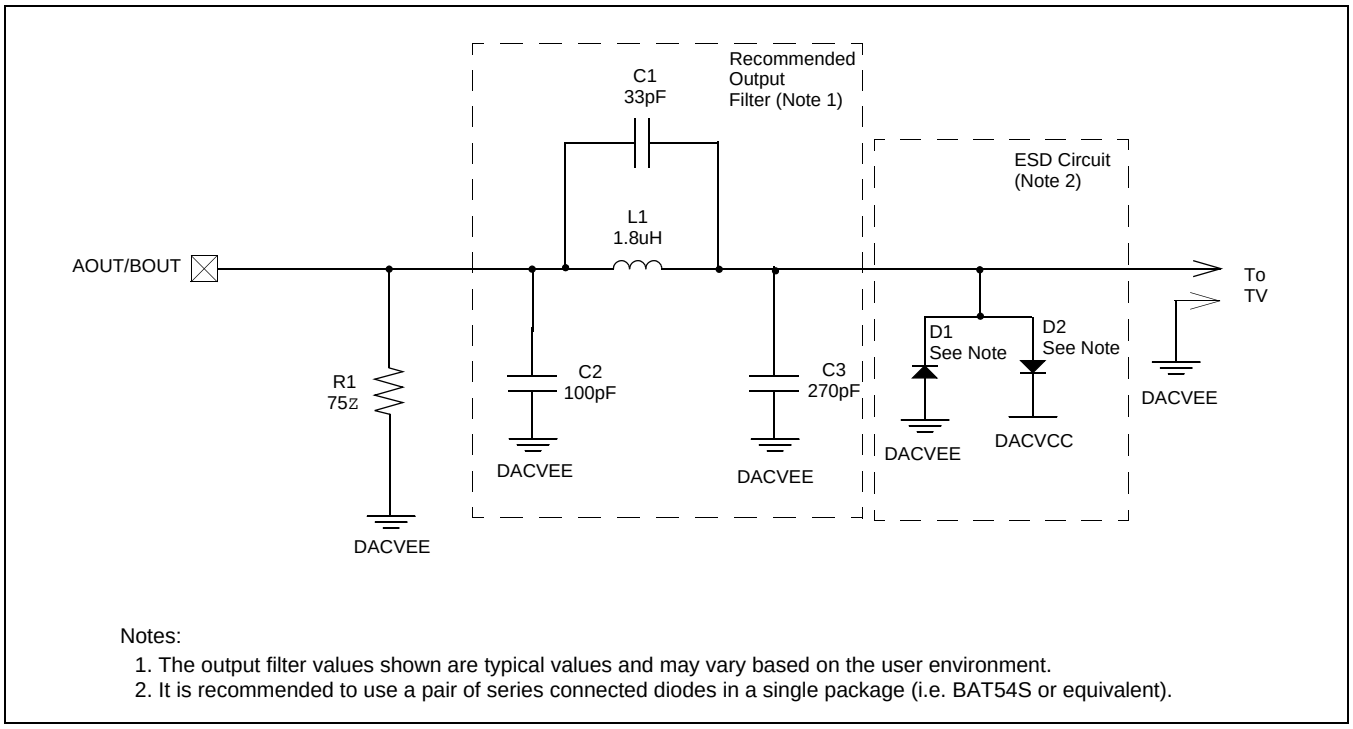


Figure 24-4: Recommended External Components - TV Output, ESD Considerations

Note

The large capacitance of the above ESD circuit may introduce minor degradation of the video signals. Typically, this degradation is not “visually” noticeable and should be evaluated for each implementation.

24.2 Crystal Oscillator Circuit

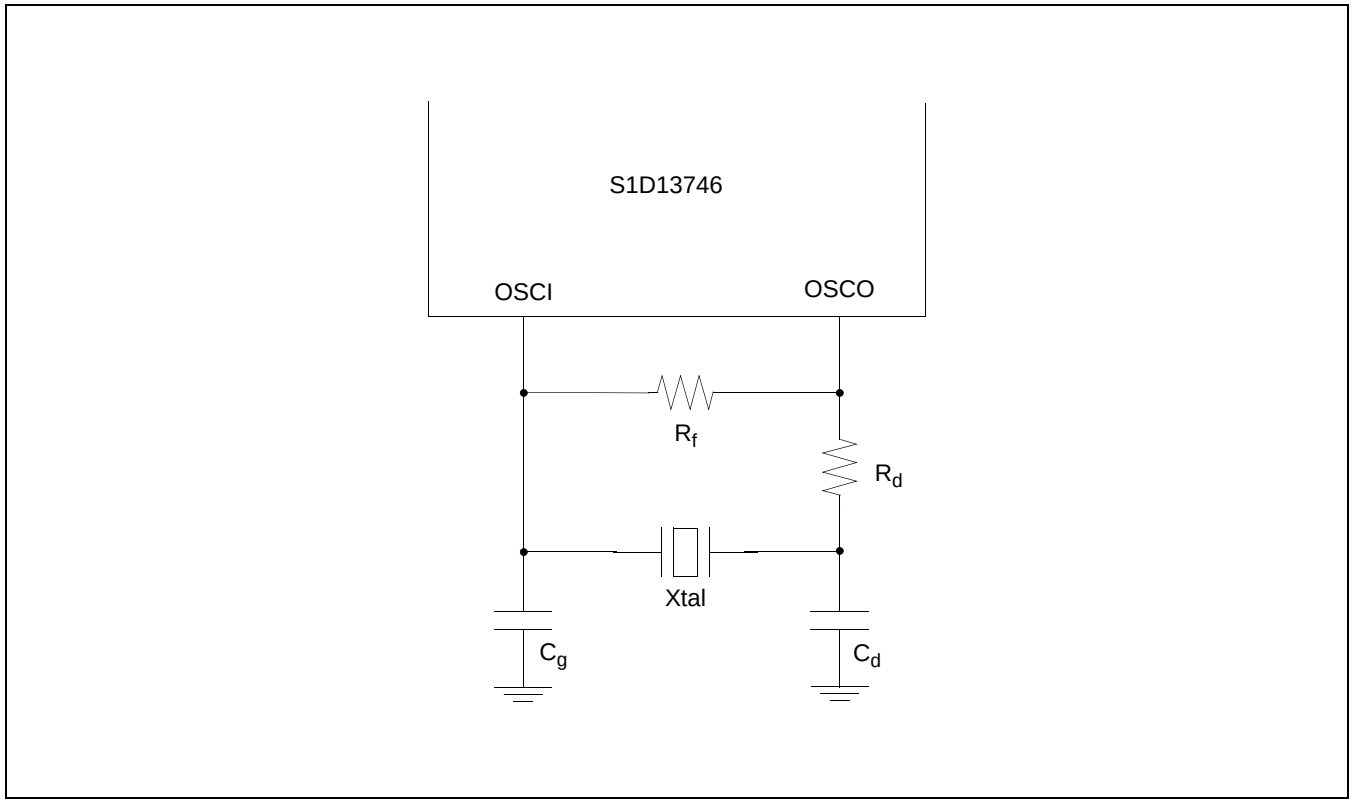


Figure 24-5: Crystal Oscillator External Circuit

Table 24-1 Recommended Oscillator External Circuit Parameter

Symbol	Parameter	Min	Typ	Max	Units
R_f	Rf	—	1	—	MΩ
R_d	Rd	—	1800	—	Ω
C_g	Cg	—	5.6	—	pF
C_d	Cd	—	5.6	—	pF
Xtal	Fundamental mode Crystal	18	27	27	MHz

25 Analog Power Supply Considerations

The PLL and DACA circuits are an analog circuit which is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of these circuits to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for these circuits to be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL and DACA circuits. This will result in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

25.1 Guidelines for Analog Power Layout

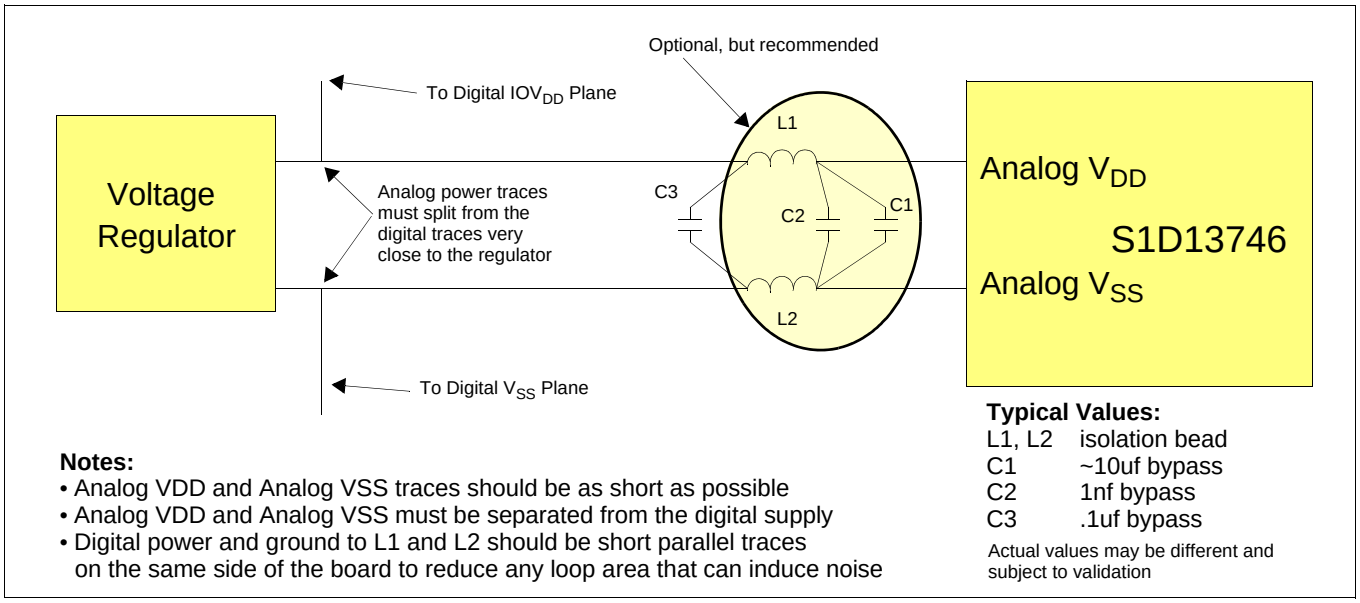


Figure 25-1: Analog Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).

- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the MGE ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.
- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

26 Mechanical Data

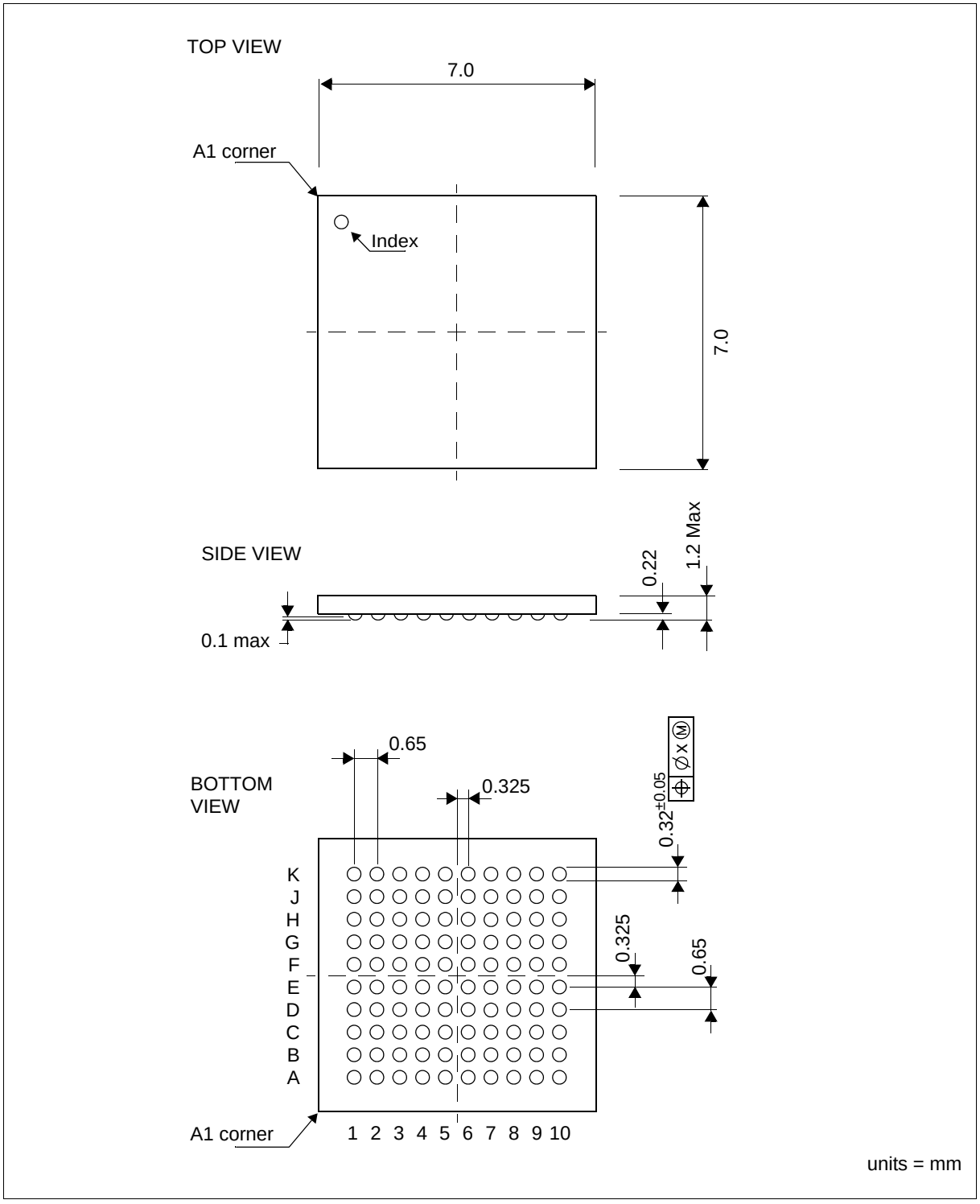


Figure 26-1: S1D13746 PFBGA 100-pin Package

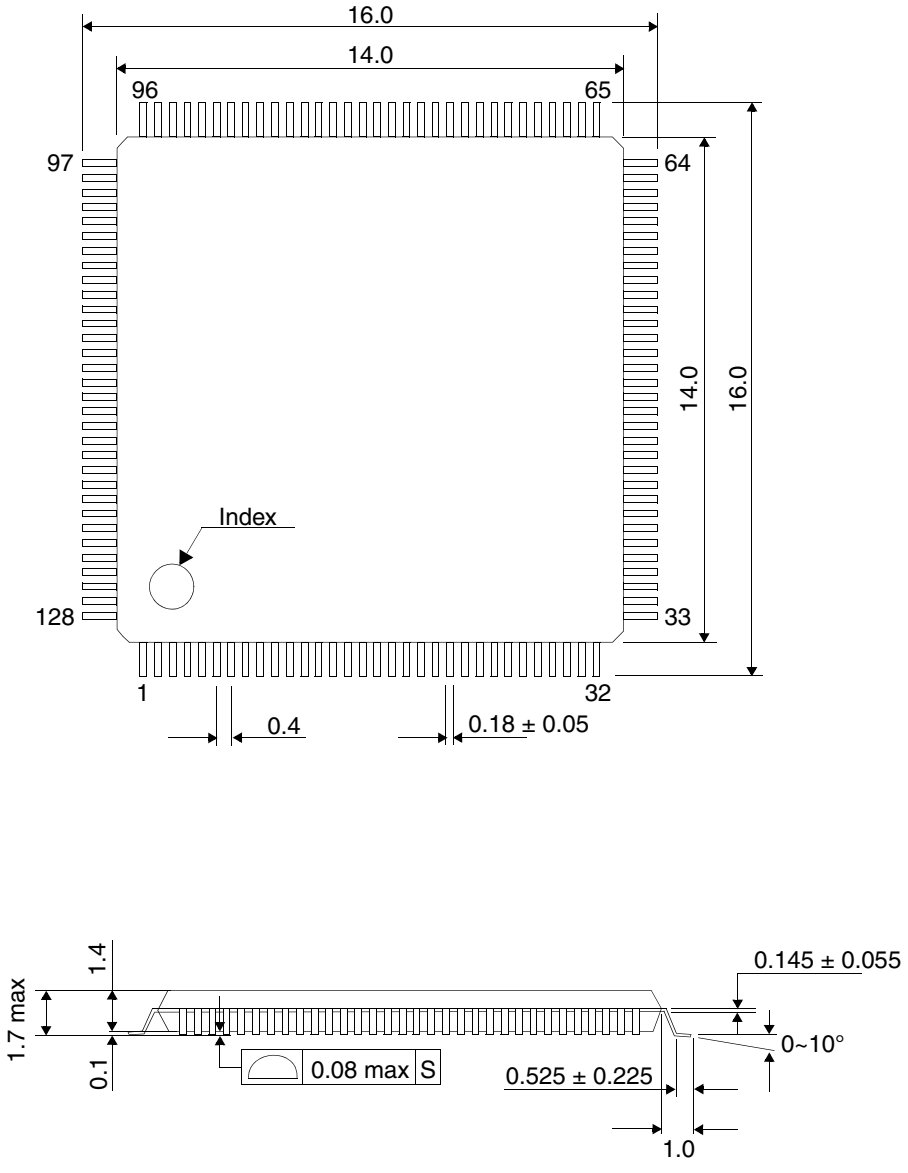
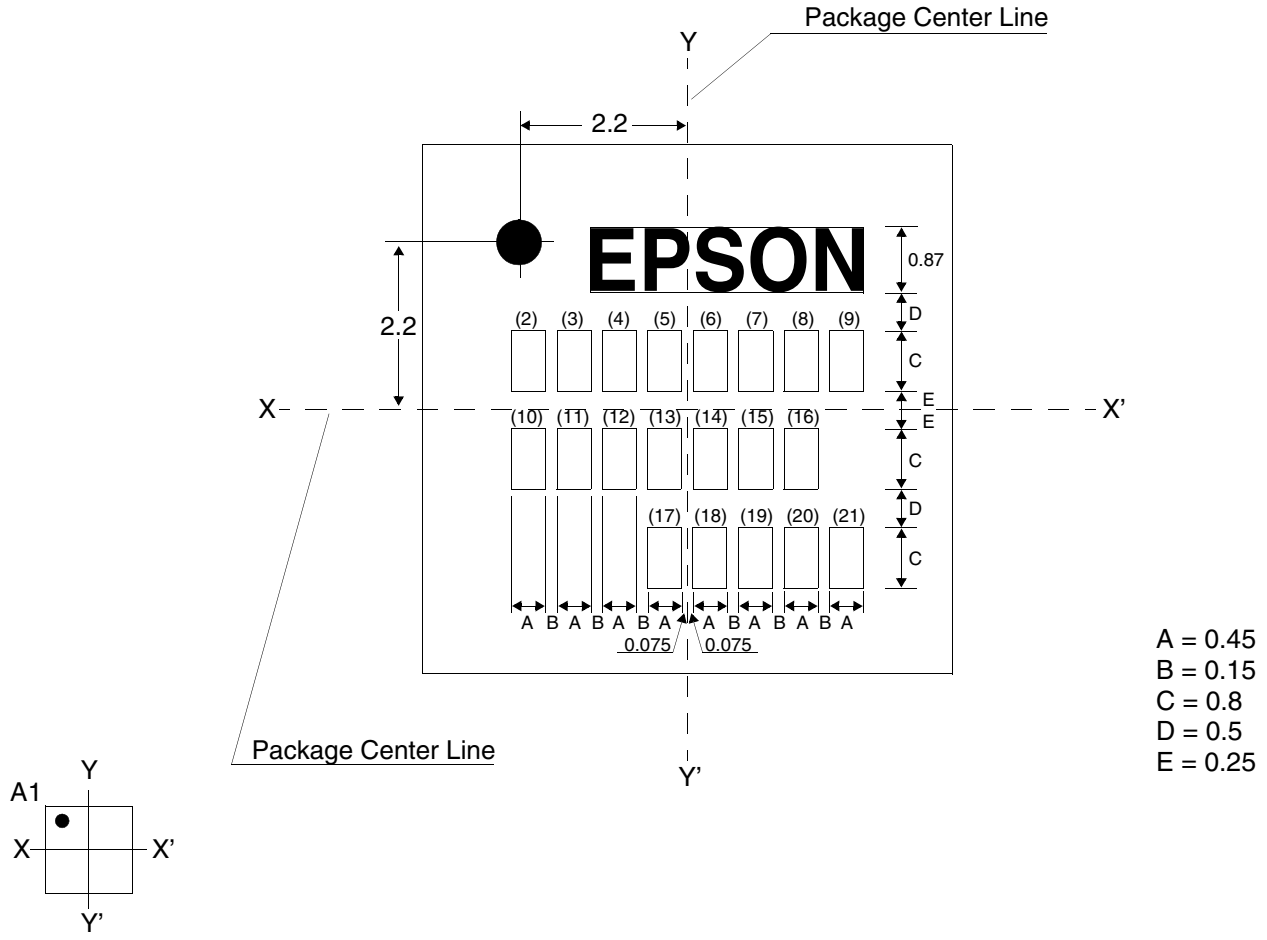
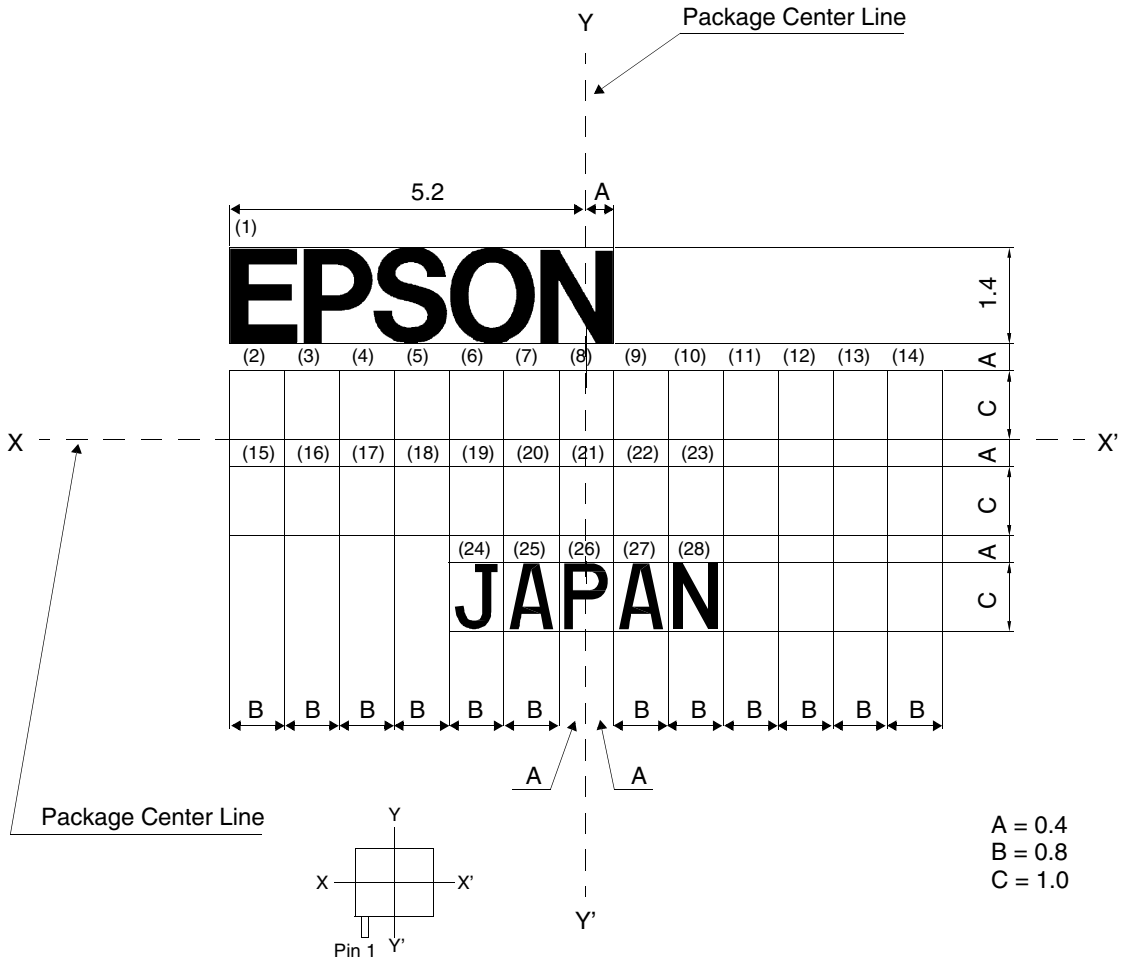


Figure 26-2: S1D13746 QFP15 128-pin Package



Item	No.	Notes
Logo Specified	(1)	
Device Name	(2) ~ (9)	137461B6
Control Code	(10))	
Year of Manufacture	(11)	Last number of A.D.
Month of Manufacture	(12)	1-9: Jan ~ Sep, X: Oct, Y: Nov, Z: Dec
Assembly Lot No.	(13) ~ (16)	
JAPAN	(17) ~ (21)	

Figure 26-3: S1D13746 PFBGA 100-pin Package Marking



Item	No.	Notes
Logo Specified	(1)	
Device Name	(2) ~ (14)	S1D13746F01A6
Control Code	(15)	
Year of Manufacture	(16) ~ (17)	Last two numbers of A.D.
Week of Manufacture	(18) ~ (19)	Calendar week of the year
Assembly Lot No.	(20) ~ (23)	
JAPAN	(24) ~ (28)	

Figure 26-4: S1D13746 QFP15 128-pin Package Marking

Table 26-1: S1D13746 Product Marking

Product Code	Marking	Description
S1D13746B01B600	137461B6	MacroVision Disabled
S1D13746F01A600	S1D13746F01A6	MacroVision Disabled

27 References

The following documents contain additional information related to the S1D13746. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13746 Product Brief (X74A-C-001-xx)
- S5U13746P00C100 Evaluation Board User Manual (X74A-G-001-xx)

28 Sales and Technical Support

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28.1 Ordering Information

To order the S1D13746 TV-Out Mobile Graphics Engine, contact the Epson sales representative in your area.

Change Record

X74B-A-001-02 Revision 2.3 - Issued: June 9, 2011

- section 8.3 RESET# Timing - changes to table 8-6 S1D13746 RESET# Timing, for t1 change Max value and remove Min value, for t2 change Min value and remove Max value
- REG[52h] bit 7 - unreserve this bit and rewrite bit description
- chapter 21 Double Buffer Description - change all occurances of “TV Frame Rate” and “TV Frame Period” to “TV Field Rate ((60Hz for NTSC and PAL-M, 50Hz for PAL)” and “TV Field Period” respectively

X74B-A-001-02 Revision 2.2 - Issued: December 11, 2008

- Changes from the previous Revision are Red
- section 8.1.3 PLL Clock - remove minimum PLL clock of 45MHz from figure 8-2 and table 8-3
- REG[42h] ~ REG[48h] - in table 11-8, VBI Data Bit Descriptions (CEI 61880, 525 Line systems), add description for VBI Data bits 1 and 0; for VBI Data bits 11 and 10, swap the descriptions for 01b and 10b
- REG[C0h] bit 1 - add note “SYSCLK must be 54MHz when 3x3 filter is enabled”
- section 16.1 3x3 Filter - add note “SYSCLK must be 54MHz when 3x3 filter is enabled”
- section 19 VBI and Wide-Screen Signalling Function - update all register references to reflect correct registers
- section 28 Sales and Technical Support - changes to offices and addresses

X74B-A-001-02 Revision 2.1 - Issued: August 5, 2008

- Changes from the previous Revision are Red
- section 8.6.2 - add this section
- REG[20h] bits 5-0 - remove note“When the input clock is between 1MHz and 18MHz or...”
- REG[2Ah] bits 6-0 - remove note 2 “When the input clock is between 1MHz and 18MHz or...”
- REG[2Ch] bit 2 - remove note “When the input clock is between 1MHz and 18MHz or...”
- REG[4Eh] bits 5-4 - remove note 4 “When the input clock is between 1MHz and 18MHz or...”

X74B-A-001-02 Revision 2.0 - Issued: September 14, 2007

- Changes from the previous Revision are Red
- add the QFP15 128-pin package information to the spec
- section 27, added References section
- section 28, added Sales and Technical Support section

X74B-A-001-01 Revision 1.05 - Issued: June 11, 2007

- Changes from the previous Revision are Red
- REG[20h] bits 5-0 - add note “When the input clock is between 1MHz and 18MHz or between 27MHz and 54MHz...”
- REG[2Ah] bits 6-0 - add note “2. When the input clock is between 1MHz and 18MHz or between 27MHz and 54MHz...”
- REG[2Ch] bit 2 - add note “When the input clock is between 1MHz and 18MHz or between 27MHz and 54MHz...”
- REG[4Eh] bits 5-4 - add note “4. When the input clock is between 1MHz and 18MHz or between 27MHz and 54MHz...” and in Table 11-13 TV Clock Settings, under CLKI Frequency, remove “27<CLKI<54”
- section 26 Mechanical Data - correct typo in figure 26-2, change “E = 025” to “E = 0.25”

X74B-A-001-01 Revision 1.04 - Issued: February 8, 2007

- Changes from the previous Revision are Red
- section 5.2.1 Intel 80 Host Interface - rewrite both PCLK and DE descriptions for connection to VSS only when not used
- section 5.2.5 Miscellaneous - rewrite PWRSVE description and add “terminated to VSS”
- section 5.2.6 Power and Ground - for OSCVSS description in table, change “IO power supply for the Oscillator (2.5v)” to “GND for the Oscillator”
- section 6.1 Intel 80 Data Pins - for MD[15:8], under 8-Bit Data, add “eight used”
- section 7.1 Absolute Maximum Ratings - correct typo in table 7-1, change “HIOVDD” to “IOVDD”
- section 7.2 Recommended Operating Conditions - correct typo in table 7-2, change “HIOVDD” to “IOVDD”
- section 7.5 Power Estimation Guidelines - in table 7-10 add S-Video output to DAC(3.0V)
- section 17.1.3 Sequential Memory Write Procedure - rewrite note “Interrupting an image frame write...”
- section 23.2 Standby Mode - in figures 23-3 and 23-4, change “Sleep” to “Standby”

X74B-A-001-01 Revision 1.03 - Issued: October 3, 2006

- Changes from the previous Revision are Red
- section 5.2.5 Miscellaneous - for GPIO[7:5] and GPIO[4:0] change RESET# State to "0"
- section 26 Mechanical Data - add figure 26-2 S1D13746 Package Marking

X74B-A-001-01 Revision 1.02 (issued 2006/09/12)

- Changes from the previous Revision are Red
- section 3.2 CPU Interface - rewrite Three Wire Serial Interface Bullet for Register data only
- section 5.2.3 TV Interface - rewrite description for AOUT, BOUT
- section 5.2.3 TV Interface - rewrite description for VADJ
- section 6.1 Intel 80 Data Pins - in table under 8-Bit Data, change MD[15:8] to Connect to ground through pull-down resistor
- section 7.3 Electrical Characteristics - in table 7-4 Power Consumption, change I_{OSC} to 600 pA
- section 7.4 DAC Characteristics - rewrite note "If the TV outputs from AOUT or BOUT are not connected..."
- section 7.5 Power Estimation Guidelines- add this section
- REG[2Ah] - replace table of example PLL clock settings
- REG[54h] bits 5-0 - rewrite bit description and change table for Common f_{timing}/f_{dds} and f_{sc}/f_{dds} Ratios
- section 20.1 Initializing the S1D13746 - add this section
- section 23.1 Sleep Mode - rewrite the first paragraph "Sleep mode disables all internal blocks..." for analog TV encoder block
- section 23.2 Standby Mode - rewrite the first paragraph "Sleep mode disables all internal blocks..." for analog TV encoder block
- section 24.1 DAC External Components - figure 24-4 Recommended External Components - TV Output, changes to the figure and added note "All component values are typical values." in figure and note "The large capacitance of the above ESD circuit..." below figure
- section 26 Mechanical Data - add table 26-1 S1D13746 PFBGA 100-pin Product Marking

X74B-A-001-01 Revision 1.01 (issued 2006/06/13)

- All changes from the previous Revision are Red
- REG[2Ch] bit 2 - un-reserve this bit

- REG[4Eh] bits 5-4 - in table 11-12 TV Input Clock Settings, reserve 11b, for table 11-13 TV Clock Settings, add TV DDS Clock Select column and 1 ƒ CLKI ƒ 18 or 27 ƒ CLKI ƒ 54 row
- section 11.3.4 Macrovision Protection Registers (REG[58h] ~ REG[5Ah]) - put these registers back in spec

X74B-A-001-01 Revision 1.0 (issued 2006/06/13)

- All changes from the previous Revision are Red
- section 3.4, added a note for the Macrovision Protection description that Macrovision is only supported when CLKI or OSC frequency is 27MHz
- section 5.2.1 Intel 80 Host Interface - for both PCLK and DE add paragraph “If the Parallel RGB Interface is not used...” to Description
- section 5.2.4 Clocks - change CLKOUT and OSCO RESET# State and Power Save State and add notes “1. When CLKOUTEN = 1, this pin...” and “2. When CNF2=1, this pin...”
- section 7.3 Electrical Characteristics - for table 7-4 Power Consumption add I_{IO} and I_{CORE} max values
- section 7.4 DAC Characteristics - add note “If the TV outputs AOUT or BOUT are not connected...”
- section 7.4, for the DAC Characteristics changed Radj from 2300ohm to 2060ohm and changed the clock cycle from 50+/-5% to 50+/-10%
- section 8.1.3, for the PLL Clock figure and table changed the maximum PLL Lock in/Stable time from 1ms to 2.5ms
- section 8.3.1, removed Memory Read parameters from the Intel 80 Timing table
- section 8.5.1, changed t3max (Vertical Active Frame Period) from “1023” to “1024”
- section 8.5.2, changed t3max (Horizontal Active Line Period) from “1023” to “1024”
- section 8.6.1 TV Output Timing - in table 8-11 Horizontal Timing for NTSC/PAL, change t1 and t5 for all, t4 = 2.52 for PAL Nc, t6 = 10.222 for PAL M, and add notes
- section 8.6.1 TV Output Timing - in table 8-11 Horizontal Timing for NTSC/PAL, change t4 = 2.52 for PAL M
- section 8.6.1 TV Output Timing - in table 8-12 Vertical Timing for NTSC/PAL, change t4 = 3 for all, and add note
- section 9.1, removed the TV DDS Clock Source Select bit from the clocks figure
- section 11.3 Register Descriptions - add paragraph “Reserved registers must not be written. The Host...” to body text
- REG[02h] bit 7 - add “...and REG[80h] bit 7 has no effect” to bit description
- REG[20h] bit 7, added information to the PLL Lock bit description that the maximum PLL Lock in time is 2.5ms and added cross reference to the PLL Clock timing section
- REG[2Ch] bit 2, reserved the TV DDS Clock Source Select bit

- REG[2Ch] bit 0 - in note change “1ms” to “2.5ms”
- REG[2Eh] - add note “IREF/VREF and TV OUT must be disabled before entering Sleep Mode”
- REG[2Eh] bit 7 - in bit description change “1ms” to “2.5ms”
- REG[2Eh] bits 1-0, added engineering text note as follows “
- REG[4Ah] bit 4 - rewrite bit description
- REG[4Eh] bits 2-0, REG[4Ch] bits 7-0, reserved the DDS Accumulator Reset Value bits
- REG[4Eh] bits 5-4, for the TV Clocks Setting bit description added option=11b where timing=26MHz and fdds=26MHz
- REG[4Eh] bits 5-4, for the TV Clocks Setting bit description added a note for option=10b when CLKI is not 26MHz as follows “If REG[4Eh] bits 5-4 = 10b and CLKI is less than 26MHz, the SCH Phase error cannot meet the consumer grade specification of within 20 degrees.”
- REG[4Eh] bits 5-4 - in table remove row starting “1 ƒ CLKI ƒ 18 or 27 ƒ CLKI ƒ 54”
- REG[4Eh] bits 5-4, for the TV Clocks Setting bit description removed references to REG[2Ch] bit 2 from the TV Clock Settings table
- REG[58h] ~ REG[5Ah] - reserve these registers. Under normal operation these registers should not be written to
- REG[62h] bit 7, for the Window Data Type bit description added cross references to the Use Case and Double Buffer sections, and removed the notes which are explained in the back sections
- REG[62h] bit 6, added double-buffer restrictions relating to the input frame rate and the input data burst when Parallel RGB interface is selected
- REG[62h] bit 6, for the Double-Buffer Enable bit description added cross references to the Use Case and Double Buffer sections, and removed the notes which are explained in the back sections
- REG[62h] bit 5, for the Background Window bit description added cross references to the Use Case and Double Buffer sections, and removed the notes which are explained in the back sections
- REG[62h] bit 5 - add note “1. For RGB Host Interface, this bit must be set to 1b”
- REG[62h] bit 4 - correct typo in table under scaling ratio for NTSC
- REG[62h] bit 4, added a note to the Square Pixel Correction Enable bit description that PALM is not supported
- REG[64h] ~ REG[6Ah], added information to the Input Window Size / Position Registers section including more input width/height restrictions and a figure/table indicating supported resolutions

- section 11.3.5 Input Data Control Registers - under Input Window Size/Position Registers in the paragraph “Depending on the background input window resolution...” change “height must be divisible by 1, 2, or 4” to “height must be divisible by 2, 4, or 8”
- REG[64h] ~ REG[6Ah], added engineering text information to the Input Window Size / Position Registers section about double-buffering restrictions based on the background window
- REG[64h] ~ REG[6Ah], added the following information to the Input Window Size/Position Description “The overlay window output x,y start positions are referenced to the background output size (size after scaling). The overlay input window size is referenced to the background input size (size before scaling).”
- REG[80h] bit 7 - correct typo in bit description, change reference to REG[04h] to REG[02h]
- REG[80h] bit 7, added a note for the Macrovision Enable bit description that Macrovision is only supported when both TV clocks are configured for 27MHz
- REG[82h] ~ REG[88h], added a note to the Display Output description as follows “The overlay window output x,y start positions are referenced to the background output size (size after scaling). The overlay input window size is referenced to the background input size (size before scaling).”
- REG[92h] ~ REG[96h], added formulas for generating the YUV values needed for the Border Color registers
- REG[98h] ~ REG[9Ch], added formulas for generating the YUV values needed for the Transparency Color registers and re-organized the bit description for clarity
- REG[98h] ~ REG[9Ch] - remove note “2. When using transparency, the input scaler is not available”
- REG[9Eh] bits 7-2 - add these bits
- REG[A0h], removed comment about “...individual memory location reads...”
- REG[A2h] ~ REG[A6h], reserved the Memory Read Address registers
- REG[ECh], changed the default register value from “06h” to “26h” for the Non-Display Period Control / Status register
- section 14.5 YUV 4:2:0 ODD Line with Intel 80, 16-bit Interface - add note “When using this mode, the input window width must be divisible by 4”
- section 16.1.1, added Dot Crawl + Flicker Filter programming values to the 3x3 Pixel Matrix Filter Function table
- section 17.1 Register Write Procedure - add paragraph “Writing to the S1D13746 registers is a two step process...”
- section 17.1, removed information about “... memory reads...”
- section 17.2 Register Read Procedure - add paragraph “Writing to the S1D13746 registers is a two step process...”
- section 17.1.3 Sequential Memory Write Procedure - rewrite section

- section 18, added double-buffer restrictions relating to the input frame rate and the input data burst when Parallel RGB interface is selected
- section 21 Double Buffer Description - rewrite entire section
- section 21, Double Buffer Description section updated with ILB information
- section 23, added new section with recommended sequences for entering and exiting sleep mode
- section 24.2, for the Crystal Oscillator Circuit table changed the Rd typical value from 820 Ohms to 1800 Ohms
- section 24.2 Crystal Oscillator Circuit - in the table add Xtal min and max values

X74B-A-001-00 Revision 0.03 (issued 2006/05/15)

- All changes from the previous Revision are Red
- section 2.1.4 Multiple TV Windows - rewrite Multiple Windows with Transparency and add the third mode “Text Mode”
- section 3.8 Miscellaneous - add package information
- section 5.1 Package Pin Mapping - add note “Pins marked as NC...”
- section 5.2 Pin Descriptions - add AP, G, and AG to Key
- section 5.2.1, for MD[7] fixed pin# typo, should be “E9” instead of “E7”
- section 5.2.1, for MD[6] fixed pin# typo, should be “E10” instead of “E6”
- section 5.2.1 Intel 80 Host Interface - rewrite GPIO_INT description
- section 5.2.3 TV Interface - for AOUT, BOUT description add “For further details...”, and rewrite the VREF and VADJ descriptions
- section 5.2.4 Clocks - add note “For details on the clock...” and change the Power Save Status for OSCO
- section 8.3.1 Intel 80 Interface Timing - in table 8-5 for twc parameter change “rising edge” to “falling edge”
- section 8.6.1 TV Output Timing - in table 8-12 Vertical Timing for NTSC/PAL change the heading “NTSC” to “NTSC M/J, PAL M” and “PAL” to “PAL B/D/G/H/I/N/Nc”
- section 9.1 Clock Block Diagram - correct error for selection of TV Timing source
- REG[2Ch] bit 2 - add “This clock should not be from...” and change “OSC or Xtal” to “CLKI or OSCx” in “When this bit = 0b...”
- REG[2Ch] bit 1 - add “or OSCx” to “When this bit = 0b...”
- REG[2Ch] bit 0 - change “OSC or Xtal” to “CLKI or OSCx” in “When this bit = 0b...” and correct typo in note, change “10ms delay” to “1ms delay”
- REG[2Eh] bit 1 - correct typo in bit description, change “10ms delay” to “1ms delay”
- REG[40h] bits 6-5 - correct typo in table, under Standard, change ITU-R BT.119-2 to ITU-R BT.1119-2

- INDEX[05h] bits 2-0 - correct typo, change 525/50 to 625/50 in equations
- REG[C0h] - correct typos in table 11-29 3X3 Pixel Matrix Filter Function Programming Values, change second set of U1 ~ U8 to V1 ~ V8
- section 12 Intel 80, 8-Bit Interface Color Formats - for each subsection add “When REG[60h] bits 3-0 =...”
- section 15.1 SwivelView Concept - correct typo, change LCD to TV
- section 16.1 Example Programming Values - correct typos in table 16-1 3X3 Pixel Matrix Filter Function Programming Values, change second set of U1 ~ U8 to V1 ~ V8

X74B-A-001-00 Revision 0.02 (issued 2006/04/07)

- All changes from the previous Revision are Red
- globally remove references to DACVDD and change DACVSS to DACVEE
- section 1.2, added YYC, YRC, RYC, VDP, VNDP, DDS, POUT to the list of abbreviations
- section 1.2.1, added Comparison section
- section 5.1 Package Pin Mapping - change pins K2 to NC and K3 to DACVEE
- section 5.2.5 Miscellaneous - rewrite the PWRSVE pin description and change cell type to HI
- section 5.2.6 Power and Ground - add pin K3 to DACVEE
- section 7 D.C. Characteristics - this entire section has been edited and updated
- section 8 A.C. Characteristics - changes to Conditions, change IOVDD range
- section 8.1.1 Input Clocks - multiple changes to table 8-1
- section 8.1.2 OSC Clock - add this section
- section 8.1.3 PLL Clock - in figure 8-2, change the PLL min = 45 and max = 54, and lock time to 1 ms
- section 8.1.3 PLL Clock - multiple changes and updates to table 8-3
- section 8.2 RESET# Timing - in table 8-3, for CNF3 = 1 change t1 min to 5.01 and max to 5.10
- section 8.3.1 Intel 80 Interface Timing - multiple changes and updates to table 8-5
- section 8.4.1 3-Wire Serial Interface Timing - in table 8-5 change t3 min to 8 and t7 max to 25
- section 8.4.2 4-Wire Serial Interface Timing - in table 8-6 change t3 min to 8, t6 max to 20, and t7 max to 25
- section 8.5.3 Input Signal Timings Relative to PCLK - in table 8-9 change t2 min to 8
- REG[62h] bit 4 - add table for bit function
- REG[ECh] bit 5, added bit state descriptions to the TE Status bit description

- REG[ECh] bit 4, added bit state descriptions to the Input Busy Status bit description
- REG[ECh] bit 3, updated the TE Output Pin Enable bit description to better describe the actual function of this bit
- REG[ECh] bits 2-0, fixed register reference typo in the table (“E8h” changed to “ECh”) and added TE Output Pin Function Timing figure
- section 17.1, for the Host Interface Access example diagrams, changed references to “D[7:0]” to “MD[7:0]”
- section 23.1 DAC External Components - figure 23-3 Recommended External - DAC Power Pins, ESD Considerations, remove references to DACVDD and DACVSS
- section 24, removed references to SAVDD and SPVDD from the Analog Power Supply Considerations section, these power supplies do not apply to the S1D13746

X74B-A-001-00 Revision 0.01 (issued 2006/03/02)

- All changes from the previous Revision are Red
- created from the S1D13745B00 specification rev. 0.12
- section 3.5 TV Display Features - add bullet “Square pixel output width scaling”
- section 3.7 Clock Source - rewrite note “An 18MHz to 27MHz clock is required...”
- section 5.2, updated HI, HIS, HID, HO, HB, and HBD cell descriptions to include “Fail Safe”
- section 9.1 Clock Block Diagram - add TV Timing Source Select and TV DDS Source Select to diagram
- section 11.1 Register Mapping - change Address F0h to FAh to “Asynchronous” in table 11-1 S1D13746 Register Mapping
- REG[00h] - change default value to A9h, change bits 1-0 value to 01b
- REG[02h] bit 7 - correct typo in bit description (register reference)
- REG[20h] - change default value to 1Ah
- REG[2Ah] - change default value to 35h
- REG[2Ah] - changes to entire PLL Setting Examples table
- REG[2Ch] - add bits 2 and 1 to register
- REG[4Ah] bit 4 - rewrite bit description
- REG[4Ch] bits 7-0 ~ REG[4Eh] bits 2-0 - add note “The value written into REG[4Ch] will not...”
- REG[4Eh] bits 7-6 - reserve these register bits
- REG[4Eh] bits 5-4 - add these bits to register
- REG[52h] bit 7 - reserve this bit

- REG[54h] bits 4-0 - changes to tables, add 2 more Luminance Filter coefficients and 4 more Chrominance Filter coefficients to tables, and add User Clock Ratio
- REG[56h] add “and User Clock Ratio” to register name
- section 11.3.5 Input Data Control Registers - under Input Window Size / Position Registers, add the paragraphs “The maximum input window resolution for...” and “Depending on the background input window resolution, the...” with table under Limitations
- REG[62h] bit 4 - add this bit to register
- REG[64h] ~ REG[66h] - add 2 bits to Input Window Height
- REG[68h] ~ REG[6Ah] - add 2 bits to Input Window Width
- REG[9Eh] bits 7-2 - reserve these bits
- section 22 TV Filter Operation - rewrite for 15 tap filter