PIC18F2682/2685/4682/4685 Rev. A1 Silicon Errata

The PIC18F2682/2685/4682/4685 Rev. A1 parts you have received conform functionally to the Device Data Sheet (DS39761**B**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2682/2685/4682/4685 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F2682/2685/4682/4685 silicon.

The following silicon errata apply only to PIC18F2682/2685/4682/4685 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2682	10 0111 000	00001
PIC18F2685	10 0111 001	00001
PIC18F4682	10 0111 010	00001
PIC18F4685	10 0111 011	00001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: ECAN™ Technology

Following an error on the bus, the ECAN module is unable to switch from Listen Only mode directly to Configuration mode.

Work around

Use the REQOP (CANCON<7:5>) bits to select Normal mode as an intermediate step, when switching from Listen Only mode to Configuration mode.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: ECAN™ Technology

Under specific conditions, the TXBxSIDH register of the pending message for transmission may be corrupted. The following conditions must exist for this event to occur:

1. A transmit message must be pending.
2. All of the receive buffers must be full and a received message is in the Message Assembly Buffer (MAB).
3. A receiver buffer must be made available (RXBxCON<RXFUL> set to '0') when a Start-of-Frame (SOF) is recognized on the CAN bus or on the instruction cycle prior to the SOF for the TXBxSIDH corruption event to occur. The timing of this event is crucial.

Work around

Ensure that a receive buffer overflow condition does not occur, and/or ensure that a transmit request is not pending, if a received buffer overflow condition does exist.

The pseudo code segment in Example 1 on the following page is an example of how to disable a pending transmission. This code is for illustration purposes only.

Date Codes that pertain to this issue:

All engineering and production devices

EXAMPLE 1:

```
If (RXBnOVFL == 1)        // Has an overflow occurred?
       {   If (TXREQ == 1)// Is a transmission pending?
           {   TXREQ = 0; // Clear transmit request
               If (TXABT == 1)// Store transmission aborted status value
                   MyFlag = 1;
           }
       }
       Temp_RXREG = RXBx; // Read receive buffer
       If (MyFlag)        // Was previous transmission aborted?
       {   TXREQ = 1;     // Set transmit request
           MyFlag = 0;    // Reset stored transmission aborted status
       }
```

3. Module: Timer1 and Timer3

When either Timer1 or Timer3 is configured to use the external clock source in 8-Bit Asynchronous mode (T1CON<7:0> or T3CON<7:0> = 0xxx x111), writes to the corresponding TMRxH:TMRxL registers may not occur as expected.

For the purposes of this issue, instructions that directly affect the contents of the Timer registers are considered to be writes. This includes CLRF, SETF and MOVF instructions.

Work around

Insert a delay of one instruction cycle between writes to TMRxH and TMRxL. This delay can be a NOP, or any instruction that does not access the Timer registers (Example 2).

EXAMPLE 2:

```
CLRF    TMR1H
MOVLW   T1Offset  ; 1 Tcy delay
MOVWF   TMR1L
```

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 3.

EXAMPLE 3: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;         //Stop timer from incrementing
PIE1bits.TMR1IE = 0;          //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                 //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;         //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);          //Wait for 2 timer increments more than the Updated Timer
                              //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                        //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;          //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;          //Now re-enable interrupt vectoring for timer 1
```

APPENDIX A: REVISION HISTORY

Rev A Document (8/2006)
First revision of this document which includes silicon issues 1-2 (ECAN).

Rev B Document (12/2006)
Updated silicon issues 1-2 (ECAN™ Technology).

Rev C Document (2/2007)
Corrected code comment in Example 1 for silicon issue 2 (ECAN™ Technology).

Rev D Document (4/2007)
Added silicon issue 3 (Timer1 and Timer3).

Rev E Document (5/2007)
Added silicon issue 4 (10-Bit Analog-to-Digital Converter).

Rev F Document (7/2014)
Updated errata to new format; Added Module 5, Timer1/3.

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